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Linearity Enhanced Noise Cancelling Low Noise Amplifier for Ultra-Wideband Application

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Abstract

The Low Noise Amplifier (LNA) stands as a crucial element RF receiver chain, demanding a delicate interplay of characteristics such as high gain, low noise figure (NF), superior linearity, and an extensive dynamic range. De-signing an ultrawideband (UWB) LNA poses a complex challenge as engineers grapple with intricate trade-offs inherent in these parameters. To address these challenges, noise cancellation techniques have emerged as valuable tools, revolutionizing the design of UWB LNAs by relaxing the traditional trade-off between bandwidth and input matching. This innovative approach not only enhances bandwidth but also effectively cancels out the un-desirable noise and nonlinearities from the input MOSFET. Despite the advancements afforded by noise cancellation, the broad bandwidth of UWB LNAs presents a significant hurdle. If the linearity is insufficient, the UWB LNA faces performance degradation due to increase in-band interference. In response, this article proposes an inventive linearization technique, a combination of Noise Cancelling (NC) and complementary derivative super-position (CDS), aiming to increase the linearity of UWB LNAs. Through meticulous simulations conducted using Cadence Virtuoso with GPDK090 library, the proposed LNA showcases impressive performance metrics across the UWB spectrum. Notably, it achieves a gain ranging from 12.5 dB to 15.5 dB, a noise figure within the range of 3.9 dB to 5.26 dB, and an IIP3 spanning from 6.3 dBm to 8.8 dBm. Remarkably, this innovative LNA accomplishes these feats while operating with a modest power consumption of 11.36 mW from a 1.2 V supply. This groundbreaking technique holds promise for significantly enhancing the efficiency and overall performance of UWB LNAs within contemporary RF receiver systems.

Keywords: Noise Cancellation; LNA-Low Noise Amplifier; CM-Current Mirror; CG-Common Gate; Linearity; Complementary; UWB-Ultrawideband.

1- Introduction

The rapid progress in communication technology necessitates fast data transmission, high-speed connectivity, and extensive bandwidth. To meet these demands, it is crucial to develop wideband RF frontends capable of supporting multiple frequency bands. Consequently, research efforts are being directed toward designing low noise amplifiers that can effectively operate across wide frequency ranges. Several researchers have put forward designs for wideband low noise amplifiers (LNAs) intended for the (3.1 GHz to 10.6 GHz) [1]–[7]. However, these LNAs often involve multiple trade-offs between desirable features such as high gain, high linearity, low noise figure, input matching, and low power consumption. Consequently, achieving a well-rounded LNA design that incorporates all these features is a challenging task [8]. For instance, while it is possible to attain high gain and low noise figure in an LNA, it typically comes at the expense of increased power dissipation, making the ultrawideband LNA power-hungry [9]. Wideband matching can be accomplished by using inductors, but this approach requires a significant amount of physical area [2]– [4] [6].

1-1- Sate of Art

To designing wideband LNAs, the most employed topologies are CG and Common CS with resistive feedback. However, these topologies often face trade-offs between input matching and NF or having a low gain and high-power dissipation. In CS with resistive feedback, the inclusion of a feedback resistor introduces extra noise and also restricts

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gain in wide-band applications [10], [11][12]. Achieving wideband input matching can be accomplished in the CG-LNA, but it comes at the expense of high-power dissipation. To address this trade-off, gm-boosting of the input device is suggested in [13]. However, the noise introduced by the gm-boosting stage results in an increased NF. NC is a commonly employed technique in wide-band LNAs, aimed at reducing input device noise by utilizing an auxiliary device, however this noise re-duction trade-off with power consumption [1-23]. To reduce the noise and power consumption of the auxiliary device in NC, two approaches, namely, dual-NC and current reuse, are introduced in [23] and [9], respectively.

1-2- Motivation

The wide bandwidth of UWB LNA permits the entry of numerous in-band interferences. In cases where the LNA's linearity is insufficient, this leads to the 2nd - 3rd order intermodulation, cross modulation, harmonic distortion (HD) and gain compression (P1dB) collectively degrade the LNA performance. Thus, LNA linearity becomes a crucial parameter, and it is defined by the input 2nd - and 3rd -order intercept points (IIP2 and IIP3). The distortion within the LNA follows a similar path as noise in an NC-LNA. Therefore, the distortion of the input device is also mitigated in the same manner as noise in an NC-LNA [1-23]. In NC-LNAs, an auxiliary device is employed to cancel the noise of the input device, forming the cascade structure in the LNA. However, in cascade structure, the presence of parasitic capacitance can lead to a degradation in linearity due to second-order interactions. Recently reported linearization techniques in [10] and [19] trade-off with bandwidth. In [17], various wideband linearization techniques are explored, and it is suggested that the integration of multiple techniques can result in better linearization. Among these techniques, CDS employs NMOS and PMOS transistors to enhance IIP3 without affecting IIP2. This method enhances linearity over a range of bias voltages rather than at a single point. Typically, the optimal biasing voltages for optimizing IIP2 and IIP3 are dis-tinct, leading to the achievement of only one optimal condition.

In this article, a hybrid linearization approach is presented, which combines NC and CDS techniques. In the CG-gm boosted NC-LNA with CM combination network, CDS is employed at both the input and gm-boosting stages to mitigate the 2nd -order interactions present in NC-LNA. This leads to enhanced linearity performance across the entire UWB spectrum.

2- Overview Of Existing NC-LNA

Low-noise amplifier's noise-cancelling principle is shown in Fig. 1, where source impedance is denoted by R_s. The idea behind noise cancellation is to locate two nodes (G and H) in the circuit where the signal and input transistor noise occur with different polarities. By using proper scaling and summation, the output signal is increased while the noise is reduced.

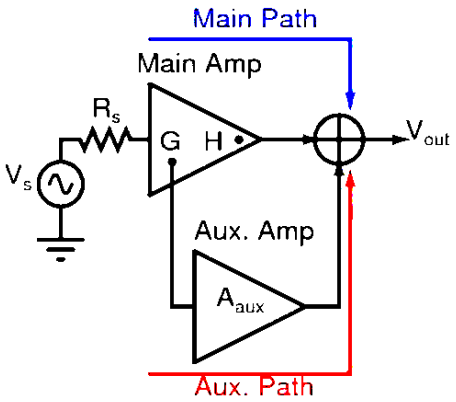

Fig. 1 Noise Cancelling Principle [8]

The CS with resistive feedback and the CG-CS topologies are the two basic ways to accomplish noise cancelling. The first topology is not well-suited for UWB applications because it exhibits limited gain and introduces higher levels of noise due to the presence of the feedback resistor [11]. The CG-CS topology provides better gain and wideband input matching than the CS with resistive feedback, making it appropriate for UWB applications [19],[25],[26]. There are numerous known NC-LNA variations based on the CG-CS topology that fall under the following categories are shown in Fig. 2. A differential output NC-LNA based on the CG-CS topology is proposed in [24], but there are numerous trade-offs between gain, bandwidth, and Noise Figure (NF). By adding another NMOS in the main path, which senses voltage and converts it to current, differential output LNA can be converted to single ended LNA to eliminate these trade-offs [17]. To obtain the current reuse output of the LNA, NMOS is substituted by PMOS in [19]. when converting a differential output to a single-ended output, the inclusion of NMOS/PMOS introduces inherent distortion, thereby compromising the linearity of the LNA. To tackle this issue, a current mirror with a mirroring ratio of N is utilized to add the signal at the output in current mode. This approach eliminates the need for voltage-to-current conversion, resulting in a reduction in distortion when compared to other CG-CS LNA [20]–[22]. The NC-LNA with current mirror combination network has input to output transconductance that is N times greater than the typical CG-CS NC LNA, which permits higher gain bandwidth products (GWB), making the NC-LNA with CM appropriate for ultrawideband applications. In NC-LNA

with CM, input device's noise/distortion is cancelled at the output when the noise cancellation condition ($N = g_{m2}R_s$) is satisfied.

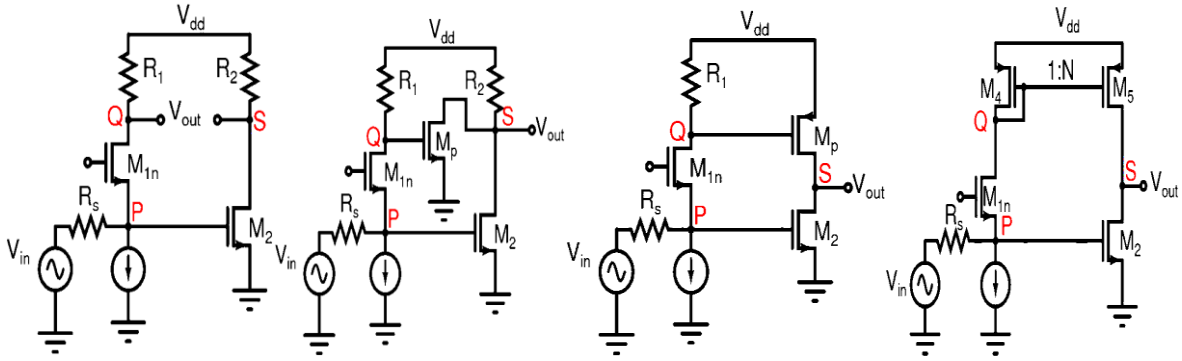

Fig. 2 (a) Differential LNA [23] (b) CG-CS single ended LNA with NMOS [16] (c) CG-CS current reuse single ended LNA [18] (d) CM-based Conventional CG-CS NC LNA [1, 5] , [19–21]

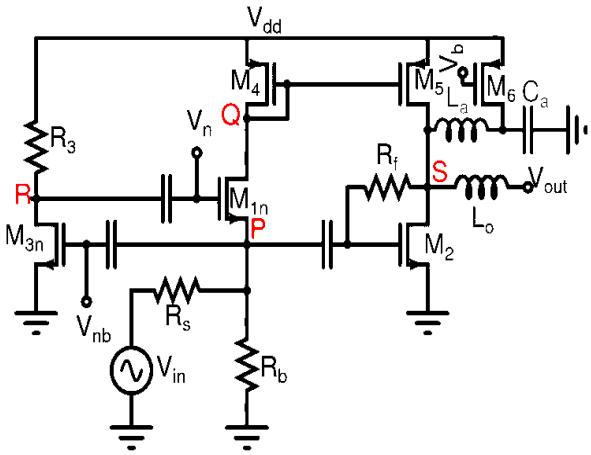

Fig. 3 g_m Boosted CG-CS-LNA incorporating a Current Mirror (CM) [5]

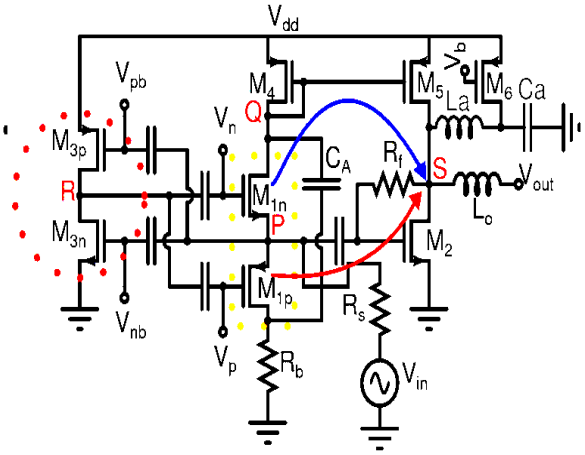

Fig. 4 Proposed CM-based CG-CS NC LNA

Additionally, the noise from transistors M_5 and M_2 can be minimized by raising the current mirroring ratio N. The remaining noise originating from M_4 in this LNA can be mitigated by decreasing g_{m4}. However, the requirement to achieve wideband input matching mandates that g_{m1} be set to 20ms, resulting in a higher current demand from M_{1n}. Since M_4 shares this same current with M_{1n}, it becomes impractical to reduce g_{m4}, ultimately designating M_4 as the primary source of noise [20]. In [1] a solution is proposed to decrease the noise from M_4 and enhance input matching flexibility. This is achieved by boosting g_m in M_{1n}, and to meet the Noise-Canceling (NC) condition, a current bleeding MOSFET (M_6) is introduced. In [5], a passive network is suggested to attenuate the noise contribution from the current bleeding MOSFET (M_6) at higher frequencies as shown in Fig. 3. Although the NC-LNA in [1], [5] offers excellent gain and noise figure, it suffers from linearity. Maximum linearity achieved in [1], [5] is -2.8 dBm @ 6 Ghz in whole UWB.

From the analysis presented earlier, it can be observed that the NC-LNA with CM exhibits the lowest distortion compared to other CG-CS NC-LNA configurations. This is because the signals are directly merged in current mode at the output. In prior works such as [1] and [5], UWB LNAs with CM have been proposed. However, their linearity is compromised, mainly due to second-order interactions. This article focused on improving the linearity of NC-LNA with CM combination network by using novel hybrid linearization technique.

3- Methods

3-1- Design Methodology

Designing a proposed wideband LNA presents several challenges, including broadband input matching and maintaining a flat gain across the frequency band. These difficulties arise due to variations in impedance and MOSFET transconductance as a function of frequency. Additionally, implementing the proposed LNA in the GPDK090 technology node introduces further challenges, such as achieving low noise and high linearity, due to the limitations of lower supply voltage and parasitic capacitance. However, the lower supply voltage helps reduce power dissipation. Despite these challenges, the higher cutoff frequency of GPDK090 makes it a viable choice for designing UWB LNA. Parasitic capacitance is characterized through S-parameter simulation. To mitigate its effects, an inductor (L_1) is placed at input to achieve wideband input matching, while two inductors ($L_a$and L_o) are placed at the output node, reducing the noise contribution of M6 and improving gain flatness across the entire bandwidth.

Implementation of the CG-CDS configuration with noise of NMOS (M_n) and PMOS (M_p) is shown in Fig. 5(a) and Fig. 5(b) respectively. while Fig. 5(c) shows the total noise of the CG complementary configuration. Capacitor C_A in Fig. 5(c) is employed to establish the AC equivalent drain node of the CG-CDS.

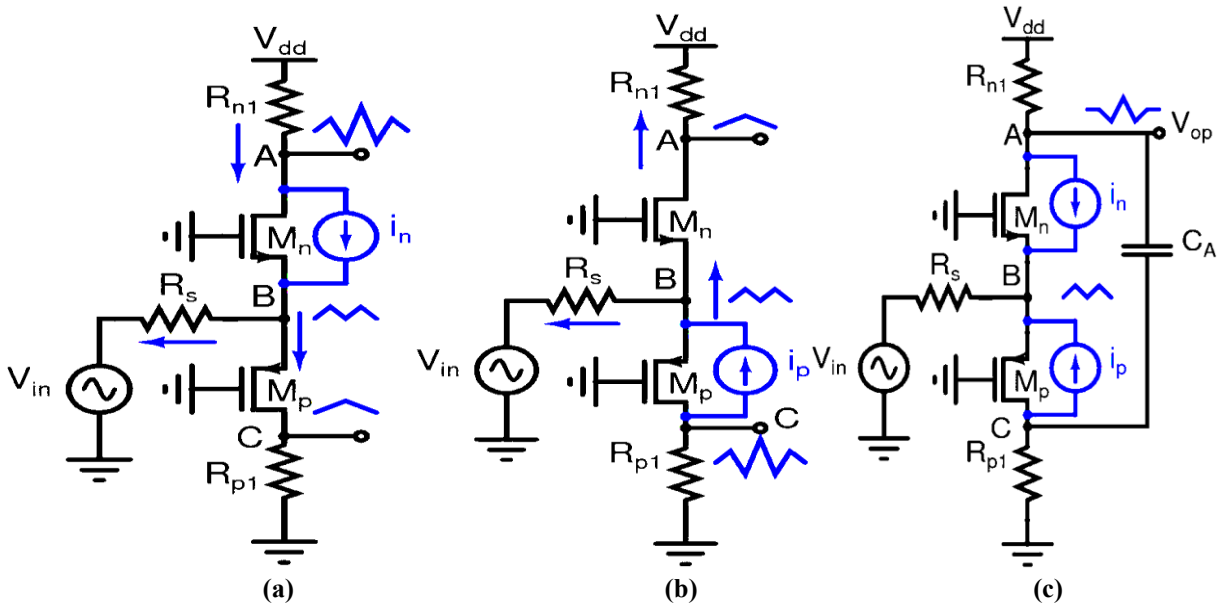

Fig. 5 (a) Noise of M_n (b) Noise of M_p (c) Toal noise in complementary common gate stage

At lower frequencies, C_A exhibits a high impedance, effectively isolating the drains of M_n and M_p, creating two separate stand-alone CG amplifiers. However, at higher frequencies, the low impedance of C_A establishes an AC equivalent drain node. Consequently, the distortion current of M_n loops back through the path of M_n-M_p-C_A-M_n. Due to the opposite g'_m profile (Fig. 7) of M_n and M_p, M_p effectively absorbs the distortion current from M_n, leading to enhanced linearity. This can also verify mathematically as in a complementary configuration, the AC input signals for NMOS and PMOS transistors are out of phase. As a result, the nonlinear output currents for NMOS (i_{dsn}) and PMOS (i_{dsp}) can be expressed as follows.

$$i_{dsn} = g_{1n}V_{gs} + g_{2n}{V_{gs}}^2 + g_{3n}{V_{gs}}^3 \quad (1)$$

$$i_{dsp} = -g_{1p}V_{gs} + g_{2p}{V_{gs}}^2 - g_{3p}{V_{gs}}^3 \quad (2)$$

The total output current (i_{out}) of the complementary configuration is then given by:

$$\begin{aligned} i_{out} &= i_{dsn} - i_{dsp} \\ &= (g_{1n} + g_{1p})V_{gs} + (g_{2n} - g_{2p}){V_{gs}}^2 + \\ &\quad (g_{3n} + g_{3p}){V_{gs}}^3 \end{aligned} \quad (3)$$

As shown in Equation 3, the second-order nonlinear coefficients (g_{2n}, g_{2p}) are subtracted at the output (Fig. 7), leading to an increase in second-order nonlinearity. Meanwhile, the third-order nonlinear coefficients (g_{3n}, g_{3p}) are added with opposite signs, resulting in a reduction of third-order nonlinearity. Consequently, the complementary configuration enhances both second- and third-order linearity.

In the presence of C_A, the percentage noise contribution from NMOS and PMOS in the CG-CDS configuration is reduced, when compared to the noise contribution at points A and B without C_A as shown in Fig. 6. In conclusion, CDS techniques can enhance linearity while also helping to reduce device noise to a certain extent.

Based on this, proposed CG-CS noise cancelling LNA in this study incorporates an active feedforward stage that replaces R_3 in Fig.3 with a PMOS transistor (M_{3p}) and introduces a PMOS transistor (M_{1p}) in the input stage to form CDS configuration as shown in Fig. 4. The cascade structure for noise cancellation can reduce linearity due to a 2nd -order interaction caused by parasitic capacitance. CDS has the capability to diminish 2nd -order interactions by lowering the 2nd-order nonlinearity coefficient of input stage. The main path incorporates a current mirror combiner (M_4 and M_5), while the NC path contains a common source stage (M_2). Additionally, a current bleeding circuit (M_6) and a biasing resistor (R_b) are utilized, where R_b can be replace with an inductor or a current source.

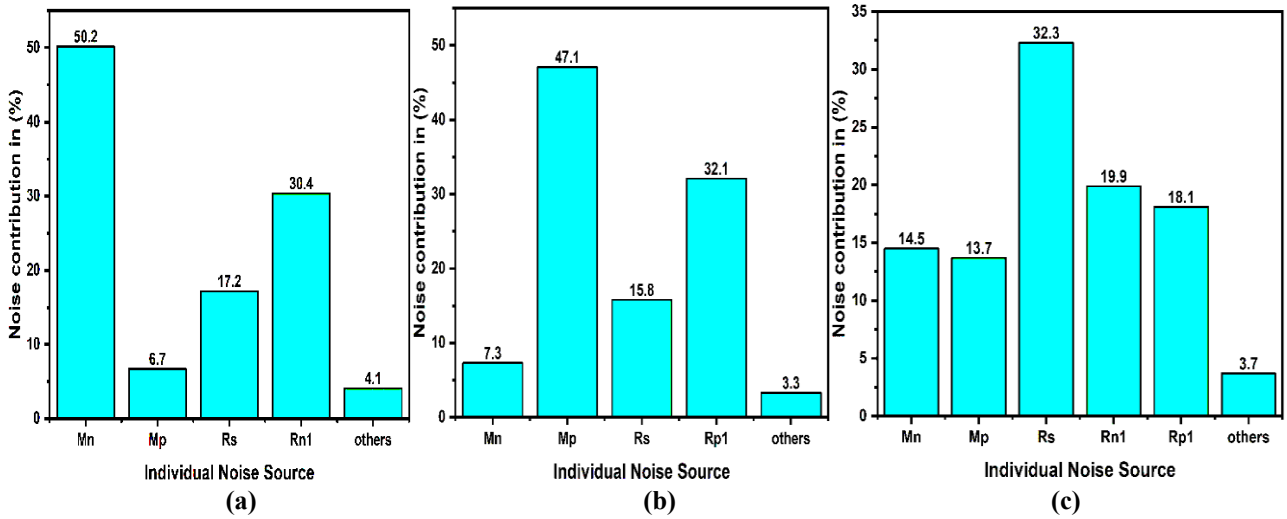

Fig. 6 Noise contribution in Fig. 5(c) at (a) Point A without CA (b) At Point B without C_A

The CM load merges the output signals originating from main and NC paths. To achieve the AC equivalent node of the complementary CG input stage (M_{1n} and M_{1p}), capacitor C_A is employed. This capacitor combines the out-of-phase noise voltages of M_{1n} and M_{1p}, leading to partial noise cancellation within the complementary CG stage. Any remaining noise of CG-CDS stage will be eliminated at the output when the noise cancellation criteria is satisfied.

The circuit operates as follows: The complementary g_m boosting stage provides input matching flexibility as well as reducing the current through M_1 and M_4. This reduction in current through M_4 lowers the gm4 results in improved noise figure and lower power dissipation. When the current through M_4 is reduced, the mirrored current through M_5 and M_2 is also reduced. This current reduction through M_2will result in a decreased g_{m2}, which will exacerbate the NC condition ($N = g_{m2}R_s$). To satisfy the NC condition, typically large g_{m2} is required. To tackle this issue M_6 is added to bleed the DC current and boost the g_{m2} [1]. However, the addition of M_6 introduces noise at higher frequencies. To address this issue, a passive network consisting of a capacitor (C_a) and an inductor (L_a) is placed at the drain terminal of M_6 [5]. Presence of parasitic capacitance at output node (S) reduce the gain at higher frequencies. To prevent this reduction in gain and to increase bandwidth, in proposed circuit includes the implementation of series peaking technique by adding inductor (L_o) at node S [15].

3-2- Input Matching and Gain

Ultra-Wideband (UWB) LNA operate over a wide frequency range (3–10 GHz), making conventional power matching challenging across all frequencies. Instead of focusing on input matching at a single frequency, the design

aims to minimize reflections across the entire band to maintain stable performance.

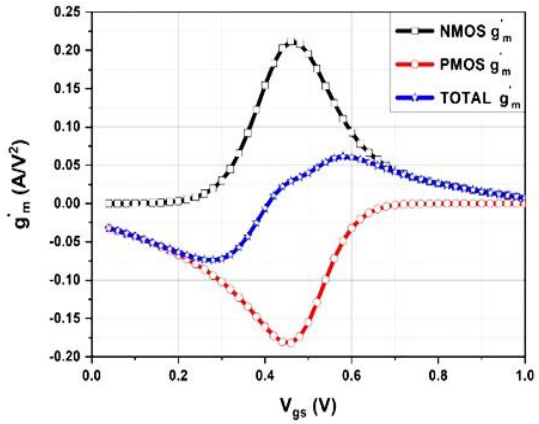

Fig. 7 g'_m profile of complementary CG stage in Fig. 5(c)

The input impedance of the suggested circuit can be represented in the following manner:

$$R_{in} = \frac{1}{g_{m1}(1+g_{m3}r_{o3})} \quad (4)$$

Where

$$r_{o3} = r_{on3} || r_{op3} \quad (5)$$

$$g_{m1} = g_{m1n} + g_{m1p} \& \; g_{m3} = g_{m3n} + g_{m3p} \quad (6)$$

The proposed circuit introduces a complementary g_m-boosting stage, which modifies the input impedance characteristics compared to conventional CG-CS LNAs with CM (Fig. 2(d)). Instead of relying solely on g_{m1}, the input impedance now depends on g_{m1}, g_{m3}, and ro_3. Consequently, achieving a 50-ohm input impedance is easily attainable by reducing the value of g_{m1} while increasing g_{m3} and ro_3. This adjustment allows for a reduction in current in the main branch, resulting in lower noise and power dissipation.

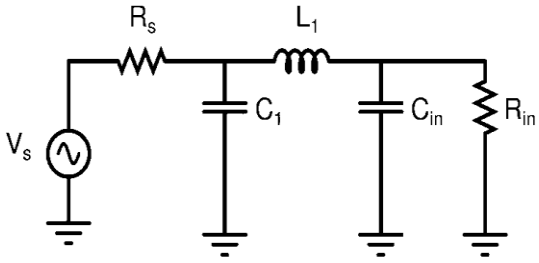

Fig. 8 π input matching [24]

Attaining effective impedance matching over a broad frequency range, particularly at higher frequencies, can be challenging due to the presence of parasitic capacitance within the input transistor. To address this challenge, the proposed circuit incorporates a π-type matching network, as shown in Fig. 8.

In Fig.8, C_{in} represents the input parasitic capacitance, while R_{in} corresponds to the impedance seen at the input of the proposed LNA. The π-type input matching network is implemented by including L_1 and C_1 components to form the necessary configuration. By using π-type matching, the circuit ensures that S_{11} remains below 10 dB across the entire ultra-wideband range. This enables effective impedance matching and maintains desirable performance throughout the entire frequency spectrum. The expression for the impedance of a π match can be formulated as.

$$Z_{in} = \frac{L_1 C_{in} R_{in} S^2 + L_1 S + R_{in}}{L_1 C_1 C_{in} R_{in} S^3 + L_1 C_1 S^2 + (C_1 + C_{in}) R_{in} S + 1} \quad (7)$$

From equation.7 wideband matching can be easily accomplished by careful optimization of the values of L_1 and C_1. The variation in L_1 and C_1 and corresponding S_{11} is shown in Fig. 13.

In Proposed circuit, gain between node P and S can be calculated by aggregating contributions from two distinct paths. In first path, input signal at node P experiences inverse amplification, resulting in an amplified signal at node R. Leveraging the substantial gate swing at the input of M_{1n}, a signal current corresponding to this is produced at node Q. This signal current is then replicated by the current mirror (CM) in the main path at a ratio of N. Simultaneously, the second (auxiliary) path directly transforms the input signal at node P into a corresponding signal current by utilizing the auxiliary CS stage. Ultimately, the two signal currents are merged at the output.

Hence, the mathematical representation of the gain from node P to node S can be expressed as:

$$A_v = -(N g_{m1}(1 + g_{m3} r o_3) + g_{m2}) R_L \quad (8)$$

The parallel output resistance r_o of transistors M_2, M_5, and M_6 contributes significantly to the overall load resistance R_L.

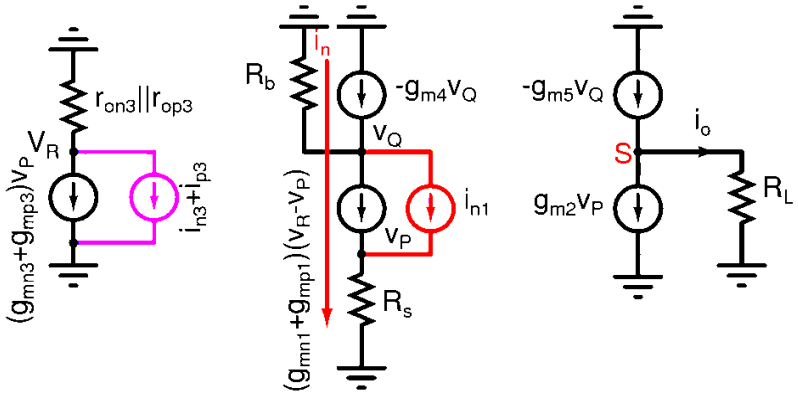

Fig. 9. Small signal modeling for analyzing noise in the suggested LNA

3-3- Noise Cancellation

The small-signal model for noise analysis of the proposed circuit is depicted in Fig. *9*. Following the partial noise cancellation within the complementary common gate stage, the noise current i_n originating from the complementary input stage gives rise to two noise voltages at nodes P and Q, exhibiting opposite polarities. Similarly, the noise current produced by the complementary g_m-boosting pair also generates noise voltages at nodes P and Q with opposite polarities. If these two noise voltages of opposite polarities are suitably adjusted in scale and then combined at the output, it becomes theoretically feasible to eliminate the noise originating from both the input and g_m-boosting stages.

Mathematically, this can be expressed as follows at the output node (S) in Fig. *9*.

$$g_{m5}v_P + g_{m2}v_Q = 0 \tag{9}$$

where,v_P and v_Q represent the noise voltages at nodes P and Q, respectively. The condition for noise cancellation can be achieved by solving Equation 9 using KCL at node v_R, v_P and v_Q.

$$g_{m2} = [g_{m1}(1 + g_{m3}r_{o3})]\, g_{m5}\left(\frac{1}{g_{m4}}||r_{o4}||R_b\right) \tag{10}$$

Where r_{04} is the output resistance of M_4. Equation.10 can be rewritten as

$$g_{m2}R_s = g_{m5}\left(\frac{1}{g_{m4}}||r_{o4}||R_b\right) \tag{11}$$

Where

$$R_s = \frac{1}{g_{m1}(1+g_{m3}r_{o3})} \tag{12}$$

Equation.11 suggests that actual noise cancellation occurs at $g_{m2} < (g_{m5}/g_{m4}\, R_s)$ due to parallel resistance of r_{04} and R_b. To evaluate the influence of R_b on NF, a set of NF plots was created for different R_b values, illustrated in Fig. *10*. Analyzing this plot allows us to determine the optimal R_b value that minimizes the NF. By considering only the channel thermal noise of MOSFETs under NC condition, the noise factor of the proposed circuit can be expressed as follows:

$$NF = 1 + \frac{\Upsilon}{N} + \Upsilon g_{m4}R_s + \frac{\Upsilon g_{m4}R_s}{N} + \frac{\Upsilon g_{m6}R_s}{N^2} \tag{13}$$

The 2nd term corresponds to the noise associated with M_2. The 3rd and 4th terms represent the noise contributions from M_4 and M_5, respectively. Reducing g_{m4} can help to reduce the noise contribution of M_4 and M_5. The

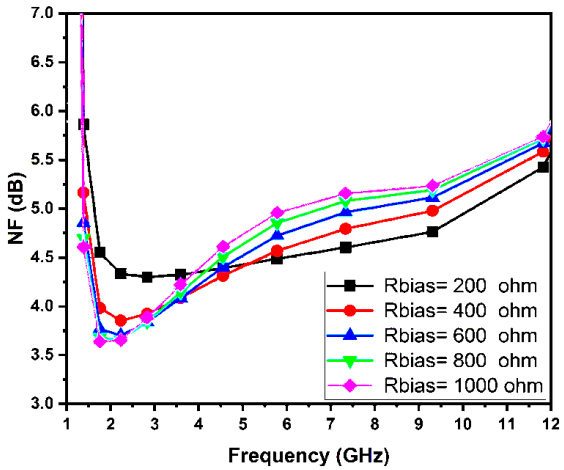

Fig. 10. NF for different value of R_b

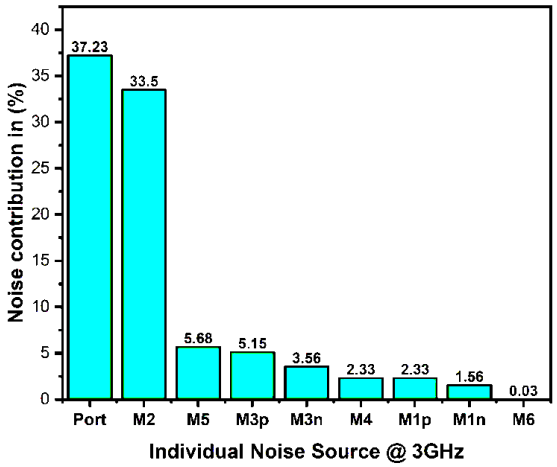

Fig. 11 Individual Noise contribution of Proposed LNA @ 3 GHz

last term denotes the noise introduced by M_6, and this noise can be reduced by employing a smaller g_{m6} and increasing the value of N. Fig. *11* illustrates the noise contributions of individual devices of proposed LNA. From this graph, after the noise cancellation, the primary source of noise is the auxiliary device (M_2). Under the noise cancellation condition, the noise from the input devices (M_{1n} and M_{1p}) and the gm-boosting stage (M_{3n} and M_{3p}) is effectively eliminated at the output. However, the inclusion of (M_{1p} and M_{3p}) to form the complementary pair introduces their own noise, which degrade NF of the proposed LNA.

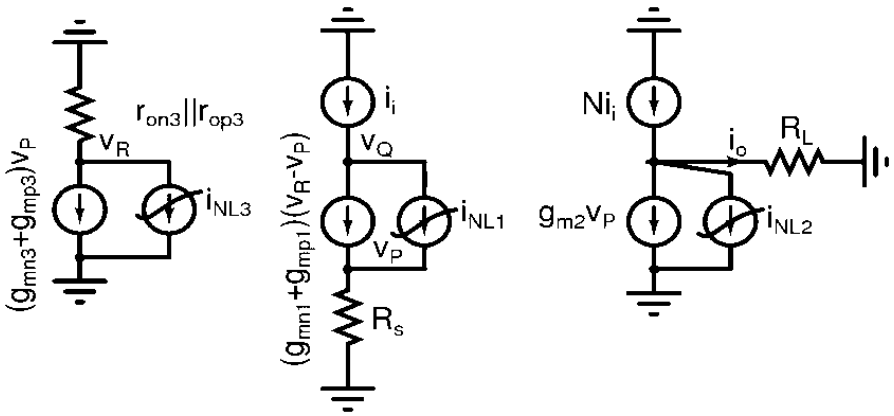

Fig. 12 Small signal modeling for evaluating distortion in the suggested LNA.

3-4- Distortion Cancellation

The nonlinearity exhibited by MOSFET can be characterized as a current source governed by V_{gs} and V_{ds} coupled to the drain and source terminals [18]. Neglecting the g_{ds}-induced nonlinearity due to output conductance.

The Taylor series can be used to depict the current source as a function of v_{gs}

$$\mathrm{i_{ds}} = \mathrm{g_m v_{gs}} + \frac{\mathrm{g'_m}}{2!}\mathrm{v_{gs}^2} + \frac{\mathrm{g''_m}}{3!}\mathrm{v_{gs}^3} + \cdots \quad (14)$$

Where

$$\mathrm{g'_m} = \frac{\partial^2 \mathrm{I_{ds}}}{\partial\, \mathrm{V_{gs}^2}},\ \mathrm{g''_m} = \frac{\partial^3 \mathrm{I_{ds}}}{\partial\, \mathrm{V_{gs}^3}} \quad (15)$$

In Fig. *12*, a small signal equivalent circuit is illustrated for distortion analysis of the proposed circuit with nonlinear current i_{NL1} , i_{NL2} , i_{NL3} of MOSFET M_1 , M_2 and M_3 respectively. From small signal Model, output current at node S can be written as:

$$\mathrm{Ni_i} = \mathrm{i_o} - \mathrm{i_2} \quad (16)$$

By using KCL at node v_R and v_P in a small signal equivalent circuit for distortion analysis (Fig. *12*) i_o can be obtained in terms of v_{in} as:

$$\mathrm{i_o} = -\mathrm{g_{m2} v_{in}} - \mathrm{g_{m2} b_1^2 v_{vin}^2} - (2\mathrm{g_{m2} b_1 b_2} + \mathrm{g_{m2} b_1^3})\mathrm{v_{vin}^3} \quad (17)$$

Where

$$\mathrm{b_1} = \frac{1}{\mathrm{a_1}} \text{ and } \mathrm{b_2} = -\frac{\mathrm{a_2}}{\mathrm{a_1^3}} \quad (18)$$

Where

$$a_1 = (g_{m1}(g_{m3}R_3 + 1)R_s + 1) \quad (19)$$

$$a_2 = \frac{1}{2}R_s(g_{m1}\mathbf{g'_{m3}}R_3 - \mathbf{g'_{m1}}(g_{m3}R_3 + 1)^2) \quad (20)$$

From the output current equation.17,3rd -order input intercept point (IIP_3) can be expressed as follows.

$$\text{IIP3} = \sqrt{\frac{4}{3}\left|\frac{g_{m2}}{2g'_{m2}b_1b_2 + g''_{m2}b_1^3}\right|} \quad (21)$$

$$2g'_{m2}b_1b_2 = 2g'_{m2} \times \left(-\frac{\frac{1}{2}R_s(g_{m1}g'_{m3}R_3 - g'_{m1}(g_{m3}R_3+1)^2)}{((g_{m1}(g_{m3}R_3+1)R_s+1))^4}\right) \quad (22)$$

Where

$$g'_{m3} = g'_{m3n} + g'_{m3p} \quad (23)$$

$$g'_{m1} = g'_{m1n} + g'_{m1p} \quad (24)$$

The Equation.21 for IIP3 clearly demonstrates that it depends on the 2nd and 3rd order nonlinearities (g'_{m2} and g''_{m2}) of the auxiliary CS stage M_2. By minimizing these nonlinearities, the IIP3 can be improved. The first term in the denominator of the IIP3 Equation, $2g'_{m2}b_1b_2$, it becomes evident that b_2 is dependent on g'_{m3} and g'_{m1} (Equation.18 & 20). However, in the proposed circuit, complementary input and g_m -boosting stage leads to reduction in g'_{m3} and g'_{m1} . This reduction in g'_{m3} and g'_{m1} directly contributes to an enhanced IIP3 for the circuit.

4- Results

To ensure a fair comparison of the proposed circuit, the g_m-boosted CG-CS LNA incorporating a Current Mirror (CM) (Fig. 3.) and the proposed circuit (Fig. 4.) were simulated using Cadence Virtuoso with GPDK090 nm CMOS process technology. In Table. 1 parameters comparison is provided for the suggested LNA and the g_m-boosted CG-CS LNA. The results reveal a noteworthy enhancement in IIP3, although there is a minor decline in terms of gain, power dissipation, and noise figure. As depicted in Fig. *13*., for π-type input matching, the values of L_1 range from 0.7nH to 1nH. Increasing the value of the inductor leads to improved input matching. In the case of the proposed circuit, a value of 1nH was chosen for L_1 because it ensures that S_{11} remains below -10dB across the entire ultrawide band. Fig. *14*. illustrates the comparison of gain between the proposed circuit and the g_m-boosted CG-CS LNA incorporating a Current Mirror (CM).

Table 1 Performance comparisons of two configurations

	Gm boosted NC-LNA with CM combination network (Fig. 3)	**Proposed LNA (Fig.4)**
Biasing condition	Resistor	Resistor
Frequency Range (Ghz)	3.1 to 10.6	3.1 to 10.6
S_{21} (dB)	16.8-23.8	12.5-15.5
NF (dB)	3.2-5.5	3.9 to 5.26
IIP3(dBm)	-4.5 to 4.3	6.3 to 8.8
Power (mW)	9	11.36

The gain of the suggested circuit is slightly lower than that of the g_m-boosted CG-CS LNA. In the entire ultrawideband range, the gain of the proposed circuit ranges between 12.5 dB and 15.5 db.

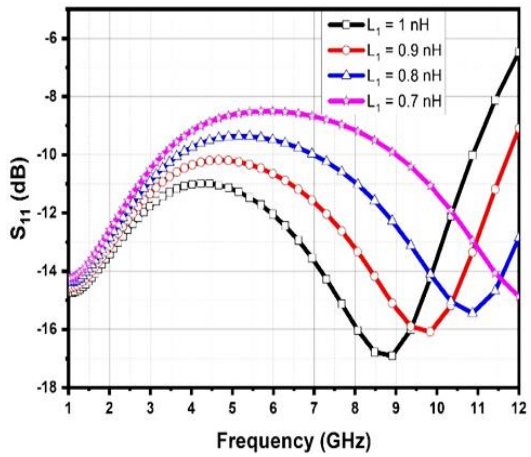

Fig. 13. S11 for Different Value of L_1

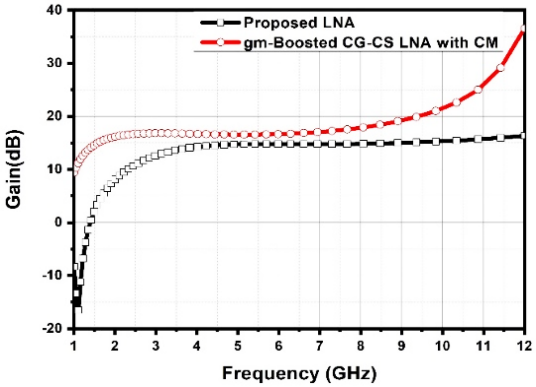

Fig. 14. Gain S_{21} (dB)

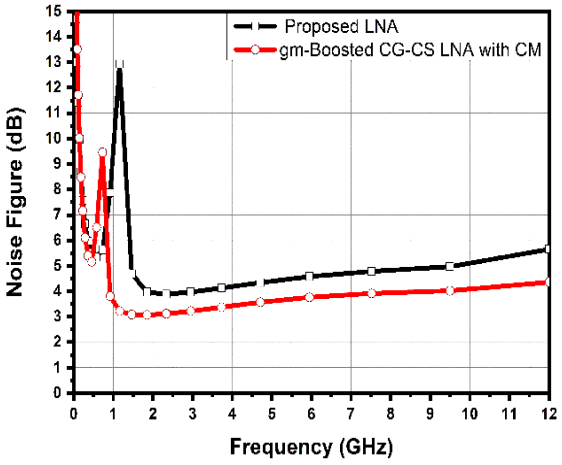

Fig. 15. Noise Figure (NF)

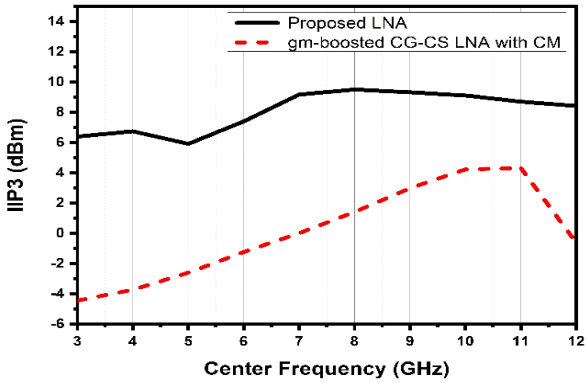

Fig. 16. IIP3 (dBm)

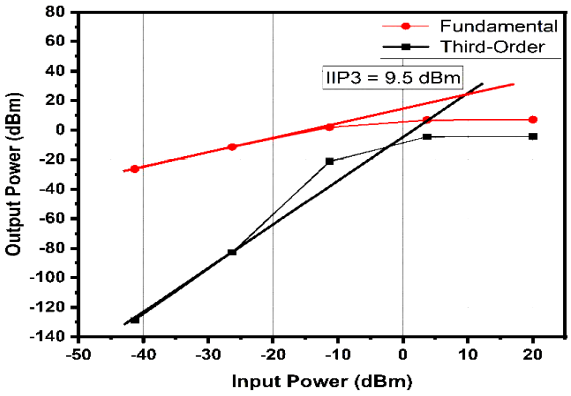

Fig. 17. IIP3 at 8 GHz

The noise of input CDS stage and g_m −boosting stage is cancelled at the output, when the noise cancellation condition indicated in Equation.10 is satisfied.NF of the suggested LNA is 3.9 dB to 5.29 dB in whole UWB, which slightly higher than the g_m-boosted CG-CS LNA as shown in Fig. *15*. However, the degradation of NF for proposed circuit is 0.24 dB to 0.7 dB, making it an appropriate choice for wideband operation.

The suggested LNA exhibits a notable improvement in IIP3 due to the cancellation of 2nd order distortion at the g_m boosting and input stage as well as reduction in 2nd order interaction. IIP3 of suggested LNA, measured at different center frequencies with a 30 MHz frequency is 6.3 dBm to 8.8 dBm in whole UWB as shown in Fig. *16.* . At the center frequency of 8 GHz, the maximum IIP3 of 9dBm is observed which is shown Fig. *17*. To assess the IIP3 performance across various frequency intervals, IIP3 is evaluated at frequency spacings of 10MHz, 20MHz, and 30MHz, as illustrated in Fig. *18*.As the frequency spacing increase, the IIP3 also exhibits a corresponding increase. The impact coupling capacitor C_A on IIP3 is also analyzed for various C_A values, and the results are depicted in Fig. *19*. It is observed that as the value of C_A increases, the IIP3 at lower frequencies also rises, due to the decreased impedance provided by C_A. To verify the sensitivity of IIP3 on biasing voltages, bias of M_{1p} (V_p) is varies from 0 to 100mv. IIP3 is notably influenced by changes in the biasing voltage, with the highest IIP3 achieved at approximately 75 mV as shown in ***Fig****. 20.*

To further evaluate the robustness of the proposed LNA, simulations are performed under process, voltage, and temperature (PVT) variations. The key LNA performance parameters are summarized in Fig. *21*. As depicted in Fig. *21*(a), input matching (S11) is not well-matched for FS and SS process variations; however, for all other PVT variations, S11 remains below -10 dB. The gain (S21) shows minimal variation across PVT conditions, as illustrated in Fig. *21*(b), while the noise figure remains below 6 dB, as shown in Fig. *21*(c). Furthermore, to assess the robustness of IIP3 under PVT variations, simulations are conducted at 8 GHz, with measurements taken across different process corners. The results in Fig. *21*(d) confirm that IIP3 remains above 0 dBm. **Table** 2. presents a comparison between the proposed work with derived simulation results from previously published wideband LNA [1], [3]–[5]. The figure of merits (FOM) [1] in Equation.25 is used to compare the performance of the suggested LNA. This FOM is well-suited for UWB LNAs as it effectively integrates critical performance factors such as bandwidth, gain, linearity, noise, and power efficiency. By placing bandwidth (BW) in the numerator, it directly accounts for wideband operation. The inclusion of IIP3 ensures linearity assessment, while (NF_min - 1) in the denominator appropriately penalizes excess noise. Additionally, P_{DC} reflects power efficiency, making the FOM ideal for low-power applications. Overall, this FOM serves as a comprehensive and practical metric for evaluating UWB LNAs, ensuring optimal functionality across the entire frequency range. Despite a modest decline in gain and noise performance, the suggested LNA achieves a high figure of merit when compared to others because of an increase in linearity.

$$FOM = 20\log_{10}\left(\frac{BW[GHz)\cdot Gain[lin]\cdot IIP3[mW]}{P_{DC}[mW]\cdot(NF_{min}[lin]-1)}\right) \quad (25)$$

In comparison to [3] and [4], the proposed circuit utilizes fewer inductors to cover the entire ultrawideband, resulting in significant physical area savings. The results demonstrate that the proposed technique enhances the linearity across the entire ultra-wideband (UWB) spectrum.

5- Discussion

5-1- Limitations

The CDS configuration enhances linearity in the proposed circuit by introducing additional PMOS in the input and gm-boosting stages, increasing circuit's complexity and contributing to noise that degrades NF. However, it also degrades LNA gain when used for IIP3 improvement, creating a IIP3 trade-off with gain and NF, as depicted in Fig. 14 and 15. To establish an AC equivalent node, a capacitor (C_A) is added in CG-CDS, increase the circuit's physical footprint. Obtaining good IIP3 in CDS relies on optimal device biasing, where g'_m approaches to zero. But this biasing is sensitive to process and temperature variations, leading to IIP3 degradation.

6- Conclusion

This article introduces an innovative method to improve the linearity of a wideband g_m-boosted CG-CS LNA. The key idea behind this approach involves the integration of a Common Source (CS) complementary pair in the g_m-boosting stage and a complementary Common Gate (CG) pair in the input stage. Accurate biasing is applied to both complementary stages, effectively eliminating second-order distortion and second-order interaction leading to a substantial improvement in linearity. Additionally, a noise cancellation principle is implemented to cancel the noise generated by both the g_m-boosting and input stages. The proposed LNA, exhibits a remarkable enhancement in linearity across the entire Ultra-Wideband (UWB) range, specifically increasing from 6.3 dBm to 8.8 dBm, when compared to the g_m-boosted CG-CS LNA. This impressive improvement positions the proposed LNA as an excellent choice for applications involving multiple interference scenarios.

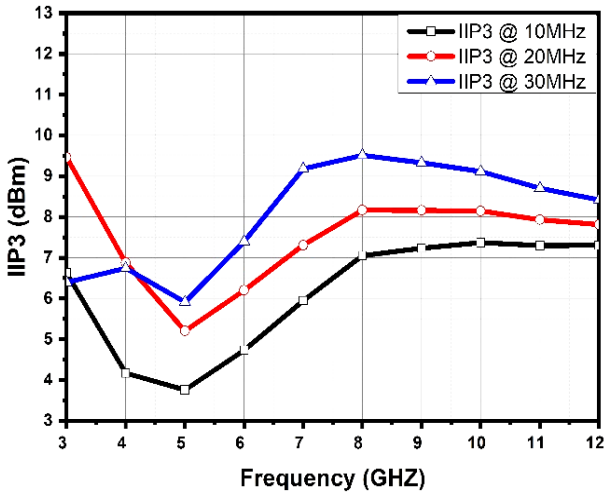

Fig. 18. IIP3 @ Frequency Spacing of 10 Mhz, 20Mhz, 30Mhz

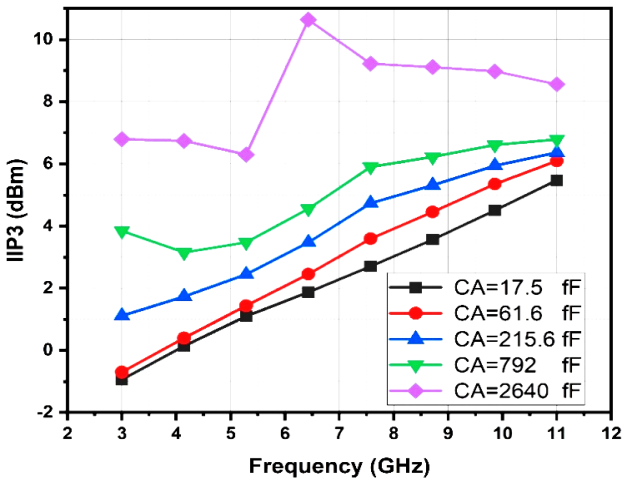

Fig. 19. IIP3 for different value of CA

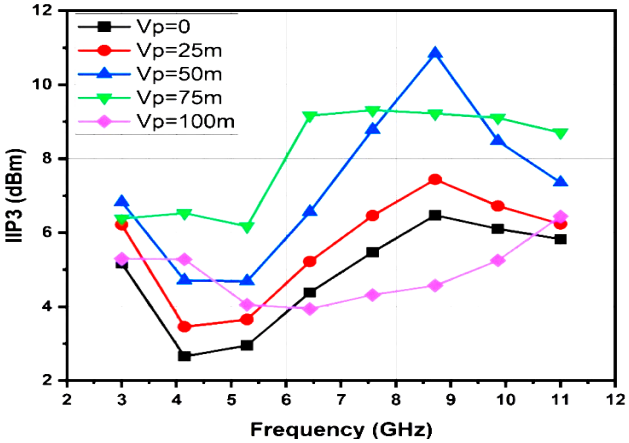

Fig. 20. IIP3 with variation in bias voltage V_p

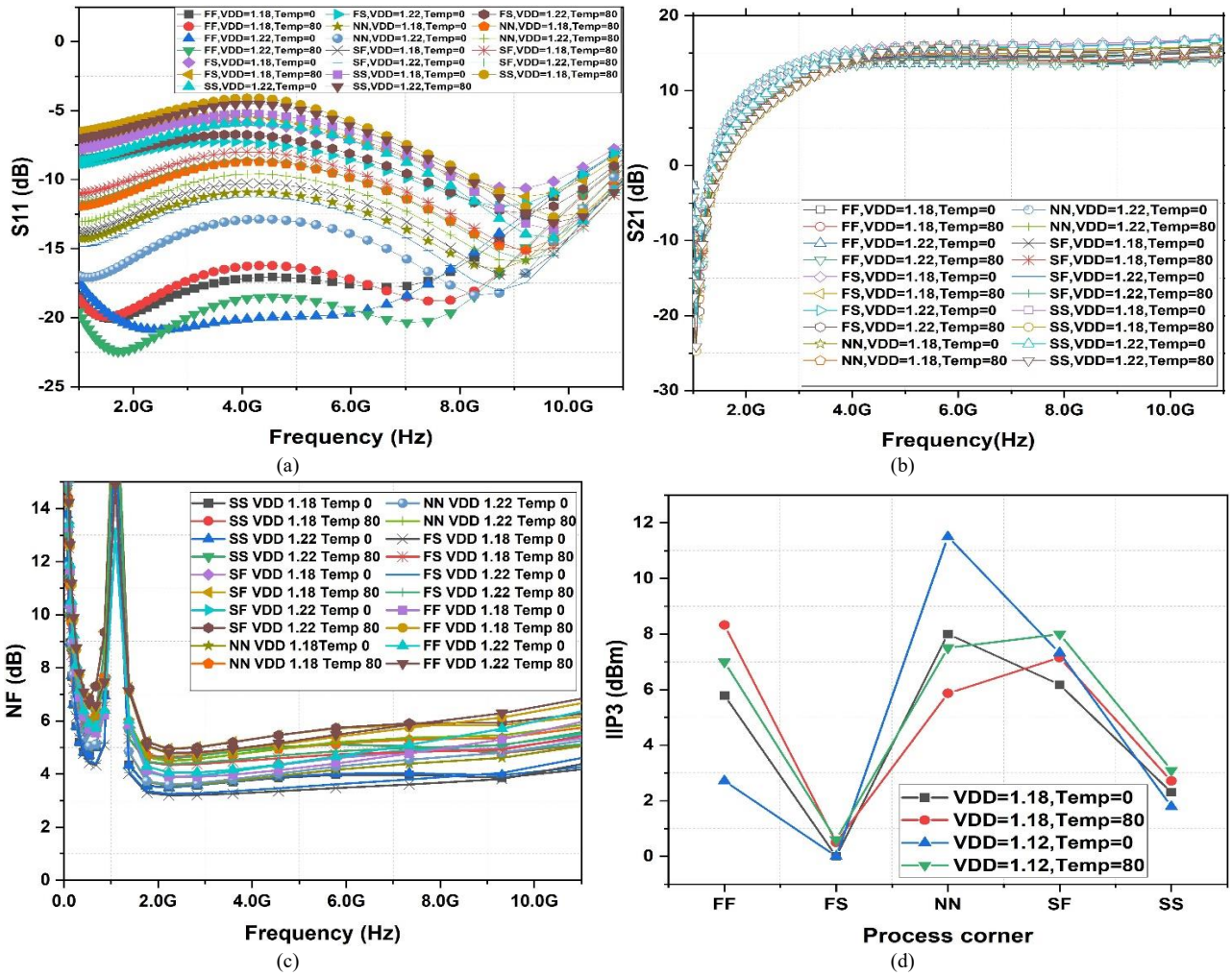

Fig. 21. PVT analysis of (a) S11 (dB) (b) Gain S_{21} (dB) (c)Noise Figure (d) IIP3

Table 2 Comparative Performance Evaluation of the Proposed Wideband LNA with Previously Reported LNAs

	S. Arshad [3]	**Q. Wan [4]**	**Z. Liu [1]**	**Z. Liu [5]**	**Proposed LNA**
CMOS Tech.	130nm	180nm	40nm	40nm	90 nm
Freq. Range (Ghz)	2.35-9.37	3.1-10.6	1-11	2-12	3.1 - 10.6
S11 (dB)	<-8*	<-10.6*	<-10*	<-10*	<-10
Gain(dB)	10.3*	15.8*	14-17*	16.5-19.5*	12.5-15.5
NF (dB)	3.68*	2.2-3.2*	3.5-5.5*	3.2-5.2*	3.9-5.26
IIP3(dBm)	-12.55*	-6*	-2.8 @ 6Ghz*	-3.5@ 6 Ghz*	9.5 @ 8 Ghz
Num. of Inductor	4	5	2	3	3
Power (mW)	9.97	9.0	9	9	11.36
Figure of Merit	-26.89	21.63	27.45	32.17	43.13

* Derived Simulation Results

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7- Future Work

Future directions, to enhance linearity through CDS techniques, include designing of robust CDS configurations that exhibit insensitivity to variations in process and temperature. Furthermore, the integration of digital control systems, advanced machine learning and AI algorithms with CDS can facilitate real-time optimization of CDS parameters which leads to better linearity.

References

[1] Z. Liu, C. C. Boon, X. Yu, C. Li, K. Yang, and Y. Liang, "A 0.061-mm21-11-GHz noise-canceling low-noise amplifier employing active feedforward with simultaneous current and noise reduction," *IEEE Trans. Microw. Theory Tech.*, vol. 69, no. 6, pp. 3093–3106, 2021, doi: 10.1109/TMTT.2021.3061290.

[2] "2.2 UWB IET Circuits Devices Syst - 2020 - Hayati - Ultra-wideband complementary metal-oxide semiconductor low noise amplifier.pdf." .

[3] S. Arshad, R. Ramzan, K. Muhammad, and Q. U. Wahab, "A sub-10mw, noise cancelling, wideband LNA for UWB applications," *AEU - Int. J. Electron. Commun.*, vol. 69, no. 1, pp. 109–118, 2015, [Online]. Available: http://dx.doi.org/10.1016/j.aeue.2014.08.002.

[4] Q. Wan, Q. Wang, and Z. Zheng, "Design and analysis of a 3.1-10.6 GHz UWB low noise amplifier with forward body bias technique," *AEU - Int. J. Electron. Commun.*, vol. 69, no. 1, pp. 119–125, 2015, [Online]. Available: http://dx.doi.org/10.1016/j.aeue.2014.08.001.

[5] Z. Liu and C. C. Boon, "A 0.092-mm22-12-GHz Noise-Cancelling Low-Noise Amplifier With Gain Improvement and Noise Reduction," *IEEE Trans. Circuits Syst. II Express Briefs*, vol. 69, no. 10, pp. 4013–4017, 2022, doi: 10.1109/TCSII.2022.3185455.

[6] H. Yu, Y. Chen, C. C. Boon, S. Member, P. Mak, and R. P. Martins, "LNA With Dual Complementary pMOS – nMOS Configuration," vol. 68, no. 1, pp. 144–159, 2020.

[7] Z. Pan, C. Qin, Z. Ye, Y. Wang, and Z. Yu, "Wideband Inductorless Low-Power LNAs with Gm Enhancement and Noise-Cancellation," *IEEE Trans. Circuits Syst. I Regul. Pap.*, vol. 65, no. 1, pp. 26–38, 2018, doi: 10.1109/TCSI.2017.2710057.

[8] B. Razavi, *RF Microelectronics (Prentice Hall Communications Engineering and Emerging Technologies Series)*, 2nd ed. USA: Prentice Hall Press, 2011.

[9] A. Bozorg and R. B. Staszewski, "A 0.02-4.5-GHz LN(T)A in 28-nm CMOS for 5G Exploiting Noise Reduction and Current Reuse," *IEEE J. Solid-State Circuits*, vol. 56, no. 2, pp. 404–415, 2021, doi: 10.1109/JSSC.2020.3018680.

[10] P. B. T. Huynh, J. H. Kim, and T. Y. Yun, "Dual-Resistive Feedback Wideband LNA for Noise Cancellation and Robust Linearization," *IEEE Trans. Microw. Theory Tech.*, vol. 70, no. 4, pp. 2224–2235, 2022, doi: 10.1109/TMTT.2021.3139331.

[11] H. Yu, Y. Chen, C. C. Boon, C. Li, P. I. Mak, and R. P. Martins, "A 0.044-mm2 0.5-To-7-GHz Resistor-Plus-Source-Follower-Feedback Noise-Cancelling LNA Achieving a Flat NF of 3.3±0.45 dB," *IEEE Trans. Circuits Syst. II Express Briefs*, vol. 66, no. 1, pp. 71–75, 2019, doi: 10.1109/TCSII.2018.2833553.

[12] J. Yan *et al.*, "A 0.2-3 GHz Inductor-Less LNA Using Noise-Canceling and Dual-Resistor Feedback Technique," *IEEE Trans. Circuits Syst. II Express Briefs*, vol. 72, no. 3, pp. 469–473, 2025, doi: 10.1109/TCSII.2025.3531994.

[13] T. Han, Z. Li, and M. Tian, "An inductor-less CMOS broadband balun gm-boosting LNA exploiting noise cancellation techniques," *Analog Integr. Circuits Signal Process.*, vol. 104, no. 2, pp. 121–129, 2020, doi: 10.1007/s10470-020-01665-2.

[14] D. Kim, S. Jang, J. Lee, and D. Im, "A Broadband PVT-Insensitive All-nMOS Noise-Canceling Balun-LNA for Subgigahertz Wireless Communication Applications," *IEEE Microw. Wirel. Components Lett.*, vol. 31, no. 2, pp. 165–168, 2021, doi: 10.1109/LMWC.2020.3042233.

[15] G. Feng *et al.*, "Pole-Converging Intrastage Bandwidth Extension Technique for Wideband Amplifiers," *IEEE J. Solid-State Circuits*, vol. 52, no. 3, pp. 769–780, 2017, doi: 10.1109/JSSC.2016.2641459.

[16] P. E. Allen and D. R. Holberg, *CMOS Analog Circuit Design*. Oxford University Press, 2016.

[17] S. Shahrabadi, "Ultrawideband LNA 1960–2019: Review," *IET Circuits, Devices Syst.*, vol. 15, no. 8, pp. 697–727, 2021, doi: 10.1049/cds2.12071.

[18] N. K. Patel and H. P. Koringa, "Systematic Analysis of Linearization Techniques for Wideband RF Low-Noise Amplifier," in *Advances in VLSI and Embedded Systems*, 2023, pp. 27–44.

[19] R. Zhou, S. Liu, J. Liu, Y. Liang, and Z. Zhu, "A 0.1-3.5-GHz Inductorless Noise-Canceling CMOS LNA with IIP3 Optimization Technique," *IEEE Trans. Microw. Theory Tech.*, vol. 70, no. 6, pp. 3234–3243, 2022, doi: 10.1109/TMTT.2022.3161279.

[20] J. Chen, B. Guo, B. Zhang, and G. Wen, "A Highly Linear Wideband CMOS LNTA Employing Noise/Distortion Cancellation and Gain Compensation," *Circuits, Syst. Signal Process.*, vol. 36, no. 2, pp. 474–494, 2017, doi: 10.1007/s00034-016-0320-9.

[21] Z. Liu, C. C. Boon, C. Li, K. Yang, Y. Dong, and T. Guo, "A 0.0078mm2 3.4mW Wideband Positive-feedback-Based Noise-Cancelling LNA in 28nm CMOS Exploiting G_m Boosting," *Dig. Tech. Pap. - IEEE Int. Solid-State Circuits Conf.*, vol. 2022-Febru, pp. 142–144, 2022, doi: 10.1109/ISSCC42614.2022.9731719.

[22] B. Guo, J. Chen, Y. Wang, H. Jin, and G. Yang, "A wideband complementary noise cancelling CMOS LNA," *Dig. Pap. - IEEE Radio Freq. Integr. Circuits Symp.*, vol. 2016-July, pp. 142–145, 2016, doi: 10.1109/RFIC.2016.7508271.

[23] A. Bozorg and R. B. Staszewski, "A 20 MHz-2 GHz Inductorless Two-Fold Noise-Canceling Low-Noise Amplifier in 28-nm CMOS," *IEEE Trans. Circuits Syst. I Regul. Pap.*, vol. 69, no. 1, pp. 42–50, 2022, doi: 10.1109/TCSI.2021.3092960.

[24] A. D. Martinez-Perez, F. Aznar, D. Flandre, and S. Celma, "Design-Window Methodology for Inductorless Noise-

Cancelling CMOS LNAs," *IEEE Access*, vol. 10, pp. 29482–29492, 2022, doi: 10.1109/ACCESS.2022.3158356.

[25] Z. Liu, C. Chye Boon, and Y. Dong, "A 0.6 V, 1.74 mW, 2.9 dB NF Inductorless Wideband LNA in 28-nm CMOS Exploiting Noise Cancellation and Current Reuse," *IEEE Trans. Circuits Syst. I Regul. Pap.*, vol. 71, no. 8, pp. 3561–3572, 2024, doi: 10.1109/TCSI.2024.3408901.

[26] M. A. Karami, M. Lee, R. Mirzavand, and K. Moez, "A 0.1-20.1-GHz Wideband Noise-Canceling gm-Boosted CMOS LNA with Gain-Reuse," *IEEE Trans. Microw. Theory Tech.*, vol. 72, no. 5, pp. 2990–3000, 2024, doi: 10.1109/TMTT.2023.3323042.