A Novel Ultra-Broad Band, High Gain, and Low Noise Distributed Amplifier Using Modified Regulated Cascode Configuration (MRGC) Gain-Cell

Zainab Baharvand*
Department of Electrical and Computer Engineering, Graduate University of Advanced Technology, Kerman, Iran
z.baharvand@student.kgut.ac.ir
Ahmad Hakimi
Department of Engineering, Shahid Bahonar University of Kerman, Kerman, Iran
hakimi@uk.ac.ir

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Abstract

In this paper, an ultra-broad bandwidth, low noise, and high gain-flatness CMOS distributed amplifier (CMOS-DA) based on a novel gain-cell is presented. The new gain-cell that enhances the output impedance as a result the gain substantially over conventional RGC is the improved version of Regulated Cascode Configuration (RGC). The new gain-cell based CMOS-DA is analyzed and simulated in the standard 0.13 μm-CMOS technology. The simulated results of the proposed CMOS-DA are included 14.2 dB average power gain with less than ± 0.5 dB fluctuations over the 3-dB bandwidth of 23 GHz while the simulated input and output return losses (S11 and S22) are less than -10 dB. The IIP3 and input referred 1-dB compression point are simulated at 15 GHz and achieved +8 dBm and -6.34 dBm, respectively. The average noise figure (NF) in the entire interest band has a low value of 3.65 dB, and the DC power dissipation is only 45.63 mW. The CMOS-DA is powered by 0.9 V supply voltage. Additionally, the effect of parameters variation on performance specifications of the proposed design is simulated by Monte Carlo simulations to ensure that the desired accuracy is yielded.

Keywords: Ultra-broad Band; CMOS Distributed Amplifier; Modified Regulated Cascode Configuration (MRGC); Low Noise.

1. Introduction

Applications of the broadband circuits in various fields such as high-rate links, high-resolution radar, imaging systems, electronic warfare, and wide band commercial or military radio systems demand a broadband amplifier as an indispensable building block at the both transmitting and receiving ends. Bandwidth increasingly becomes a controlling factor in radio frequency (RF) circuit design. Distributed amplifier (DA) is highly interested component at the high-speed amplification applications as a result of its inherent broad bandwidth, good linearity, and low sensitivity to process variations [1-4]. Distributed amplification is a method to absorb the parasitic capacitances of transistors which are main factor to restrict the bandwidth.

A simplified schematic of customary DA is shown in Fig. 1. As it can be seen, it has a pair artificial transmission lines (TL) and several active devices. The artificial gate and drain TLs essentially are constructed of series on-chip inductors in conjunction with shunt parasitic gate and drain capacitances (C_{gs},C_{ds}) of MOS transistors. The gate line is used to travel down the input signal to excite each of the active devices, in turn. Similarly, the drain line is utilized to get the desire output peak pulse through summing each of these pulses together, after amplification by active devices.

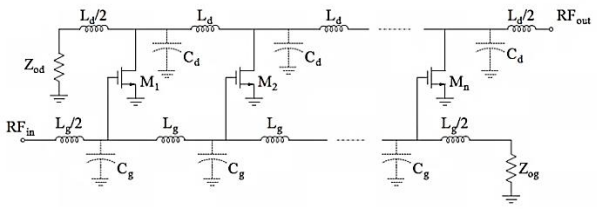


Fig. 1. The simplified circuit schematic of a conventional DA [4]

Previously reported DAs are designed into several classes, to date. DAs based on cascaded gain-cell increase the amplifier's gain while operating at low voltage and low power conditions. However, this group suffers from poor closed loop stability and lack of an ultra-broad band response, due to the incurrence of multiple poles by cascaded stages [5-8]. Another class adopts a cascode cell that is more desirable to decrease the Miller effect and to improve the reverse isolation. The voltage headroom's limitation of cascode structures makes it difficult to meet low power and high gain requirements, simultaneously. Hence, the DAs based on this group of gain-cells are unsuited to the low supply voltage applications [9]. The third class introduces two-dimensional DAs, such as cascaded single-stage distributed amplifier (CSSDA) [10], matrix DA [11], combination of the conventional

* Corresponding Author

distributed amplifier (CDA) and CSSDA [2], cascaded multi-stage distributed amplifier (CMSDA) [12, 13], and DA with cascaded gain stages [14]. This class applies the multiplicative gain mechanism to meet the high gain performance. Although this group has higher gain-bandwidth performance than other, their huge chip size and power dissipation aren't desire.

In this study, a CMOS-DA based on a new gain-cell configuration is designed to overcome the shortcomings of the previous DAs. It introduces one structure that can satisfy the combination of the most important design targets in DA designing, in terms of high power gain, broad bandwidth, low NF, and reasonable DC power consumption, simultaneously.

Additionally utilizing of Monte Carlo (MC) simulations, the parameters variation's effect on the performance specifications of the proposed design is investigated. The MC simulation results confirm that in spite of considering the tolerance effects particularly fluctuations in MOS parameters, which are unavoidable in practice, and supply voltage variations in designing the proposed DA can meet to its expected specifications. Following this introduction, Section 2 presents the analysis, design and characterization of the proposed DA. Section 3, demonstrates the simulation results. Finally, section 4 draws conclusion of the work.

2. Basic Principle of Proposed DA

Fig. 2 shows the circuit topology of the proposed CMOS-DA which is composed of three stages Modified Regulated Cascode Configuration (MRGC) gain-cell.

A summary of systematic design dividing in four steps is explained first, and these steps are then applied to design the proposed DA, as detailed in following.

Step 1) choose the optimum number of stages

Since both gate and drain artificial lines have limited quality factors, they are lossy in practice. The range of optimum number of stages reported for various DAs is between three and five. Therefore in this design to meet low power and high gain requirements, number of stages is calculated in optimum mode to be three stages.

Step 2) propose the suitable gain-cell

A new gain-cell configuration is designed to overcome the shortcomings of the previous DAs. New gain-cell based CMOS-DA alleviates the defects of the CMOS-DAs based on cascaded gain-cells, in the point of restricted bandwidth. Also, it overcomes to defects of two dimensional DAs including high power dissipation and big chip area. These advantages obtain without any limitation in the power-supply voltage and signal-swing requirements that are unavoidable in CMOS- DAs based on cascode gain-cells [6,7,9,15]. The design methodology describes in the sub-section 2-1, in detailed.

Step 3) choose the transistor aspect ratio

To avoid the bandwidth deterioration due to the pole associated to the internal node of the proposed gain-cell whose value is $P_{int,node} = \frac{g_{m2}}{(C_{i2}+C_{o1})}\left(\text{also}, P_{int,node} = \frac{g_{m3}}{(C_{i3}+C_{o4})}\right)$, the $M_2\,(\text{also}, M_3)$ transistor's transconductance value must be increased. This demands increasing the $M_2\,(\text{also}, M_3)$ transistor's width $(W_2(\text{also}, W_3))$. On the other hand, increasing $W_2(\text{also}, W_3)$ leads to increase the input capacitance $(C_{i2}(\text{also}, C_{i3}))$ of $M_2\,(\text{also}, M_3)$. The competing requirement for $W_2(\text{also}, W_3)$ in the numerator and denominator of $P_{int,node}$ implies that an optimal width for $M_2\,(\text{also}, M_3)$ exists. A bandwidth-enhancing inductor $L_n\,(\text{also}, L_m)$ is added to the source of $M_2\,(\text{also}, M_3)$ which other benefit of it is to improve the $M_2\,(\text{also}, M_3)$ transistor's transconductance. This effect arises from the fact that employing $L_n\,(\text{also}, L_m)$ enables us to raise the transistor aspect ratio and earns the objective transconductance while the similar bandwidth is obtained, at the same time. From simulation and bandwidth compensation method the optimal value for $W_2(\text{also}, W_3)$ was found to be larger than $W_1(\text{also}, W_4)$.

Step 4) choose the size L_n, L_m

For the selected transistor aspect ratio, the bandwidth-enhancing inductor $L_n\,(\text{also}, L_m)$ through simulation is adjusted to be around 0.64 nH to maximize the flat bandwidth of the propose gain-cell.

The next sub-section elaborates the effect of MRGC upon increasing the output impedance as a result increasing the gain. Also, it shows how large effect is obtained over conventional RGC.

2.1 Modified Regulated Cascode Configuration (MRGC)

Negative feedback is a known method which is greatly utilized in electronic systems design, particularly in amplification applications. There are many advantages achieved with a suitable introduction of negative feedback, in terms of: bandwidth enhancement, modified output impedance and unconditional stability [16]. This subsection presents a step-by-step approach to reach the MRGC cell that enhances RGC cell's gain.

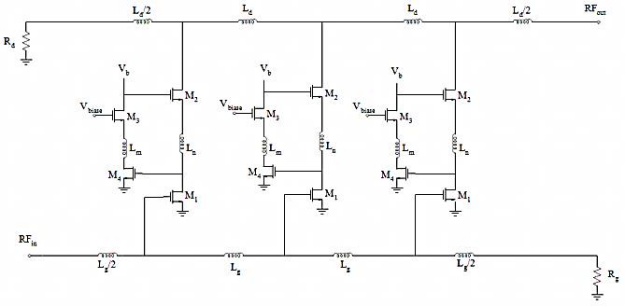


Fig. 2. The circuit topology of the proposed CMOS-DA

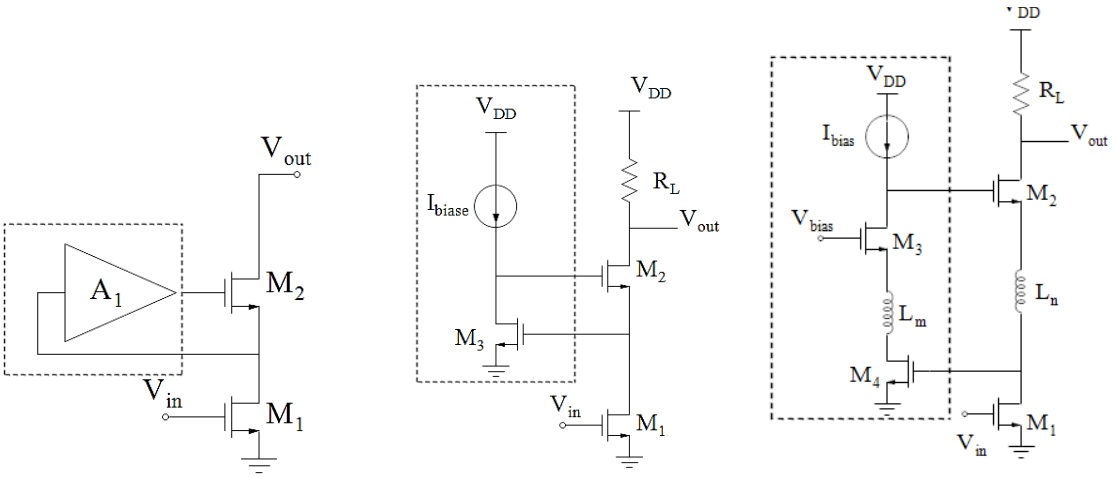


Fig. 3. a) Gain boosting in the cascode stage [17], and b) the conventional Regulated Cascode Configuration [17], and c) the Modified Regulated Cascode Configuration

Fig. 3 (a) shows the block diagram of RGC cell. In the point of calculating the R_{out} , M_1 device acts as a degeneration resistor. This device senses the output current and modulates it to a voltage signal. Now, the small signal voltage appears on the drain of M_1 device is proportional to the output current. This result suggests that the mentioned voltage can be subtracted from the gate voltage of M_2 transistor to insert this device at the current-voltage negative feedback. In fact, the A_1 amplifier forces the drain voltage of M_1 to be equal to the gate voltage of M_2. In this way, A_1 implements the negative feedback loop. The current-voltage negative feedback modifies the output

impedance as a result enhances the gain performance without stacking more cascode elements on top of M_2 transistor. Also, it increases the bandwidth and improves the stability behavior of the amplifier [16, 17]. One can prove that the voltage gain (A_v) of the RGC amplifier is given by Eq. (1) [17]:

$$A_v = -g_{m1}R_{out} \;\&\; R_{out} \approx (A_{vA1})g_{m2}r_{o1}r_{o2} \qquad (1)$$

As it shown in Fig. 3 (b), in the original case of RGC, the A_1 amplifier implements by CS cell. The output resistance

(R_{out}) and the voltage gain (A_v) of the conventional RGC amplifier are given by Eqs. (2), (3) [17]:

$$R_{out} = g_{m2}g_{m3}r_{o1}r_{o2}r_{o3} \qquad (2)$$

$$A_v = -g_{m1}g_{m2}g_{m3}r_{o1}r_{o2}r_{o3} \qquad (3)$$

Where $g_{m1,2,3}$ and $r_{o1,2,3}$ are the transconductance and the output resistances of the $M_{1,2,3}$ transistors, respectively. From the Eq. (1), it can be seen that one can increase the amount of R_{out} by increasing the value of A_{vA1} to achieve higher gain. This effect was used in designing of the proposed MRGC cell towards increasing output impedance as a result gain to that of the conventional RGC. MRGC replaces the CS cell with cascode amplifier in negative feedback loop as shown in Fig. 3(c), so it boosts the value of A_{vA1} . As a consequence, the output impedance significantly boosts over conventional RGC. It obtains in the fact that cascode cell's gain is higher than CS cell's gain. Hence, the higher gain performance of the proposed MRGC is guaranteed. Cascode cell not only illustrates higher gain to that of the CS cell, but also presents excellent reverse isolation. Also, the broader bandwidth operation can be obtained tanks to remove the Miler effect of the CS amplifier in the traditional RGC by this replacing. The output resistance (R_{out}) and the voltage gain (A_v) of the proposed MRGC amplifier can be derived to prove that the further gain can be achieved in comparing to the simple RGC:

$$R_{out} = g_{m2}g_{m3}\,g_{m4}r_{o1}r_{o2}r_{o3}r_{o4} \qquad (4)$$

$$A_v \approx g_{m1}g_{m2}g_{m3}\,g_{m4}r_{o1}r_{o2}r_{o3}r_{o4} \qquad (5)$$

As it is evident of the above equations the small-signal voltage gain of the proposed MRGC amplifier is similar to the gain of traditional quadruplet cascode amplifier while the limiting power-supply voltage and signal-swing requirements that are unavoidable in the conventional quadruplet cascode amplifier are removed. Note the parasitic capacitances in this theoretical analysis are ignored for simplicity, they are taken into account in high frequency transconductance ($G_{mt}(s)$) analysis of the proposed CMOS-DA.

To suppress the cascode cells dominant pole at higher frequencies, two bandwidth-enhancing inductors (i.e. L_m, L_n in Fig. 3(c)) are added to the proposed gain-cell. This compensation method results in high-frequency gain peaking at the drain of $M_{1,4}$ if bandwidth extension without power consumption penalty is desired [14].

2.2 High Frequency Transconductance Analysis

Fig. 4 shows MRGC gain-cell and its high frequency small-signal equivalent which is used to calculate the high frequency transconductance $G_{mt}(s)$. Calculating of $G_{mt}(s)$ is necessary because according to the CS based DA's power gain and voltage gain formulas with assuming lossless TL, $G_{mt}(s)$ is only unknown factor to

calculate the DA's power gain and voltage gain for every DA's architecture which is shaped based on a new gain cell [18]. $C'_{GS1,2}$,$C'_{DB1,2}$ are the equivalent parasitic gate-to-source, and drain-to-bulk capacitances of the $M_{1,2}$ transistors in MRGC cell, respectively. In this analysis for simplicity, it is supposed that C_{GDi} from $M_{1,2}$ devices combines with its C_{GSi} and C_{DBi} as a result of utilizing the Miller effect to shape $C'_{GS1,2}$, $C'_{DB1,2}$. Also, $g_{m1,2,3,4}$ and $r_{o1,2,3,4}$ are the transconductance and the output resistances of the MOS devices. Note that $r_{o1,2,3,4}$ are relatively large, so they can be ignored. $G_{mt}(s)$ of the MRGC cell can be derived as follows:

$$G_{mt}(s) = \frac{I_{out}}{V_{in}}(s) = \frac{I_{out}}{V_{ds1}}\frac{V_{ds1}}{V'_{ds1}}\frac{V'_{ds1}}{V_{in}} \quad (6)$$

Before of calculating the $G_{mt}(s)$, the gate-source voltage of M_2 (v_{gs2}) is determined. The gate voltage of $M_2$to ground is equal to the drain-source voltage of M_1 (v_{ds1}) which is amplified by the small signal voltage gain of A_1, that is named $(-a)$. Thus, v_{gs2} is calculated according to Eq. (7):

$$v_{gs2} = v_{g2} - v_{s2} = v_{g2} - v_{ds1} = -(a)v_{ds1} - v_{ds1} = -(a+1)v_{ds1} \approx -av_{ds1} \quad (7)$$

Also, the gate-source voltage of M_4 as evident from Fig. 4 (a) is equal to v_{ds1}. With a KCL at the output node:

$$\frac{I_{out}}{V_{ds1}} = -(ag_{m2} + g_{mb2}) \quad (8)$$

Also, from KVL at the pass of V'_{ds1}, L_n and V_{ds1}, the value of V_{ds1}/V'_{ds1} is given by Eq. (9):

$$\frac{V_{ds1}}{V'_{ds1}} = \frac{1}{SL_n(ag_{m2}+g_{mb2})+1} \quad (9)$$

Finally, With a KCL at the V_{ds1} node V'_{ds1}/V_{in} is given according to:

$$\frac{V'_{ds1}}{V_{in}} = \frac{-g_{m1}}{L_n(ag_{m2}+g_{mb2})+SC'_{DB1}} \quad (10)$$

As a consequence:

$$G_{mt}(s) = \frac{I_{out}}{V_{in}}(s) = (ag_{m2} + g_{mb2}).\frac{1}{SL_n(ag_{m2}+g_{mb2})+1}.\frac{g_{m1}}{L_n(ag_{m2}+g_{mb2})+SC'_{DB1}} \quad (11)$$

Where in Eq. (11), a defines as the high frequency small signal voltage gain of A_1 amplifier that is cascode amplifier in the proposed design and calculates according to Eq. (12) [19]:

$$\frac{V'_{out}}{V'_{in}} = -\frac{g_{m4}{g^{-1}}_{m3}\left(\frac{S^2}{\omega^2_{n,z}}+\frac{2\xi_z}{\omega_{n,z}}S+1\right)}{\left(\frac{S^2}{\omega^2_{n,p}}+\frac{2\xi_p}{\omega_{n,p}}S+1\right)}$$

$$= -\frac{g_{m4}{g^{-1}}_{m3}(L_m C_{i,3}S^2+g_{m3}L_m S+1)}{({g^{-1}}_{m3}C_{i,3}S+1)L_m C_{o,4}S^2+{g^{-1}}_{m3}(C_{i,3}+C_{o,4})S+1} \quad (12)$$

Where $C_{i,3,4}$, $C_{o,3,4}$ are the equivalent input and output parasitic capacitances of the $M_{3,4}$transistors in MRGC cell, respectively. Not that, for simplicity of high frequency analysis the small-signal equivalent circuit of cascode amplifier placed in a dashed box in Fig. 4 (b).

2.3 The Frequency Response of Noise

The noise characteristic of MESFET DAs has been analyzed in [20], and the analysis has been adapted for MOSFET DAs in [4]. The intrinsic noise sources of DA can be identified as noise from the source, gate-termination, and drain-termination resistors (R_s, R_g, R_d). Also, the transistors have two noise sources including drain current noise and gate-induced noise [21]. The noise figure of an N stage DA can be given as Eq. (13) [22]:

$$F = 1 + \frac{P_{ngT}+P_{ndT}+P_{no}}{P_{ns}G_F} \quad (13)$$

Where P_{ngT}, attenuating by the reverse gain of the DA, presents the output noise power contribution of the gate-termination resistor according to Eq. (14):

$$P_{ndT} = KT\Delta f G_F \left|\frac{\sin N\theta}{N\theta}\right| \quad (14)$$

P_{ndT}, calculating as Eq. (15), is the output noise power because of the drain-termination resistor.

$$P_{ndT} = KT\Delta f \quad (15)$$

P_{ns}, amplifying by the DA's forward gain G_F, refers to output noise power of source resistor. Finally, P_{no} shows the output noise power due to the noise sources of transistors in the k-th stage of an N stage DA, and it can be calculated as Eq. (16):

$$P_{no} = 4KTG_{mt}R_d\frac{\gamma}{\alpha}\Delta f\sum_{k=1}^{N}\left|\frac{\sin\frac{\theta}{2}}{\theta}+\frac{1}{4}G_{mt}R_gF_cM(k)\right|^2 + \frac{1}{4}KT{G_{mt}}^2G_u{R_g}^2R_d\Delta f\sum_{k=1}^{N}|M(k)|^2 \quad (16)$$

Where K and T are the Boltzmann constant and the absolute temperature, respectively. α is the ratio of gain cell's transconductance to zero-bias drain conductance which it is about 0.85 in deep-sub-micrometer MOSFETs. Also, $G_{mt}(s)$ refers to the high frequency transconductance of the proposed DA. Finally, G_u, F_c , $M(k)$, are as following:

$$M(k) = \left(N - k + \frac{1}{2}\right) + \frac{\sin\left(k-\frac{1}{2}\right)\theta}{\theta}e^{-j\left(k-\frac{1}{2}\right)\theta} \quad (17)$$

$$G_u = \delta\frac{\omega^2{C_{gs}}^2}{5g_{do}}(1-|c|^2) \quad (18)$$

$$F_c = j|c|\sqrt{\frac{\delta}{5\gamma}}\frac{\omega C_{gs}}{g_{do}} \quad (19)$$

It should be noted that the channel drain noise (i_{nd}) and the induced gate noise (i_{ng}) because of their same physical origin are correlated with a correlation coefficient defined as c. Therefore, i_{ng} decomposed into 2 parts which one is correlated with i_{nd} that is $i_{ngc}(= F_c i_{nd})$ and another completely uncorrelated that is $i_{ngu}\left(=\sqrt{4KTG_u\Delta f}\right)$. Also, δ and γ are the coefficients of gate noise and channel noise which based on the measured results in [17] they are about 4.1 and 2.21, respectively.

Substituting the above Eqs into Eq. (13) the total noise power of DA yields as Eq. (20):

$$F = 1 + \left|\frac{\sin N\theta}{N\theta}\right|^2 + \frac{4}{N^2 {G_{mt}}^2 R_g {}^2 R_d {}^2} + \frac{16}{N^2 G_{mt} R_g}\frac{\gamma}{\alpha}\sum_{k=1}^{N}\left|\frac{\sin\frac{\theta}{2}}{\theta} + \frac{1}{4}G_{mt}R_g F_c M(k)\right|^2 + \frac{1}{N^2}G_u R_g \sum_{k=1}^{N}|M(k)|^2 \quad (20)$$

Eq. (20) can be further simplified by assuming large values of N. In that case

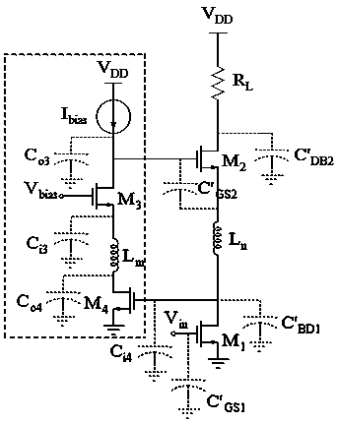
$$\sum_{k=1}^{N}|M(k)|^2 \approx \sum_{k=1}^{N}\left|\left(N - k + \frac{1}{2}\right)\right|^2 = \frac{N^3}{3} \quad (21)$$

$$\sum_{k=1}^{N}\left|\frac{\sin\frac{\theta}{2}}{\theta} + \frac{1}{4}G_{mt}R_g F_c M(k)\right|^2 \approx N\left(\frac{\sin\frac{\theta}{2}}{\theta}\right)^2 + \frac{1}{16}{G_{mt}}^2 {R_g}^2 |F_c|^2 \frac{N^3}{3} \quad (22)$$

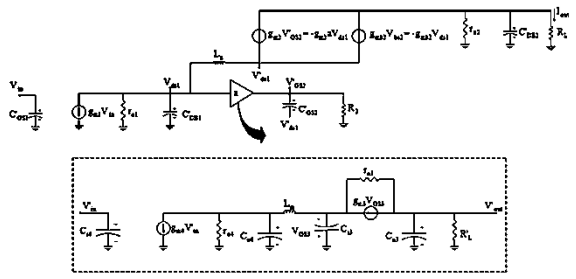
The second and third terms in Eq. (20) can be ignored for large N. Following the above supposes, the noise figure expression of DA can be given as Eq. (23):

$$F = 1 + \frac{1}{NR_g}\frac{4\gamma}{\alpha} + \frac{1}{G_{mt}}\left(\frac{\sin\frac{\theta}{2}}{\frac{\theta}{2}}\right)^2 + NR_g\frac{\alpha\delta}{3}\frac{\omega^2 {C_{gs}}^2}{5G_{mt}} \quad (23)$$

As it can be seen from Eq. (23), the noise figure expression of DA is inversely proportional to the high frequency transconductance of the proposed DA (i.e. G_{mt}), so the second and third parts of Eq. (23) can be reduced with increasing G_{mt}. Note the correlation between the gate and drain noise current sources essentially removes in Eq. (18) in the fact that $|c|^2 \ll 1$. Hence, the last term in Eq. (20) was ignored.



(a)



(b)

Fig. 4. a) Modified Regulated Cascode Configuration (MRGC) gain-cell in conjunction with parasitic capacitances, and b) the high frequency small-signal equivalent circuit of the MRGC gain-cell

3. Simulation Results

The proposed CMOS-DA is simulated using BSIM3 transistor models via Advanced Design System (ADS) simulation tool. Fig. 5 illustrates the simulated results of the power gain (S_{21}) and revers isolation (S_{12}) of the proposed CMOS-DA. As it can be seen, the flat and high gain response of 14.2 ± 0.5 dB with 3-dB bandwidth of 23 GHz is achieved. In addition, the revers isolation between input and output terminals is better than – 20 dB. The corresponding simulated results of input and output return losses (S_{11}, S_{22}) are shown in Fig. 6. Both S_{11} and S_{22} are better than −10 dB over the entire 3-dB bandwidth of 23 GHz. The simulated NF is presented in Fig. 7. As it is evident, the maximum value of NF is below 4.6 dB within the whole corresponding bandwidth while the average NF is as low as 3.65 dB.

The valuable measure of the stability is called rollett stability factor (or K-factor). If K-factor is greater than one, it implies that the amplifier is unconditionally stable [23]. As it can be seen from Fig. 8, the K-factor of the proposed CMOS-DA is bigger than unity which it shows this amplifier is unconditionally stable over range of interested frequencies from DC up to 23 GHz. The input third intercept point (IIP3) is simulated at 15 GHz. The proposed CMOS-DA achieves the good linearity performance whit IIP3 value of + 8 dBm as shown in Fig. 9. Also, simulated input referred 1-dB compression point at 15 GHz is illustrated in Fig. 10 which it achieves the value of -6.34 dBm.

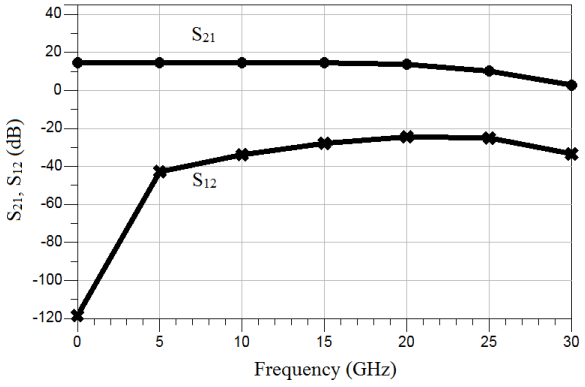


Fig. 5. Simulated results of power gain and revers isolation (S21, S12)

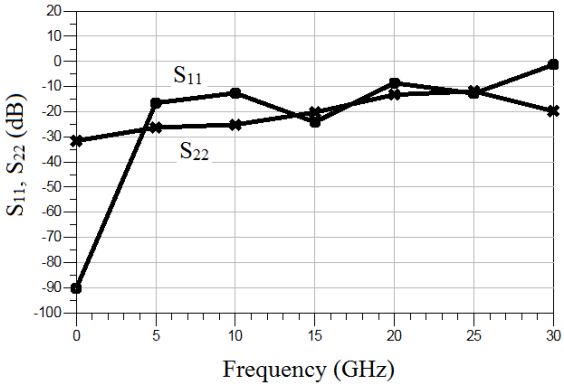


Fig. 6. Simulated results of input and output return losses (S11, S22)

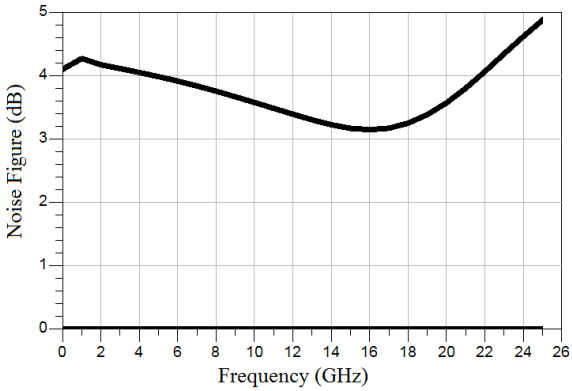


Fig. 7. Simulated noise figure (NF) of the proposed CMOS-DA

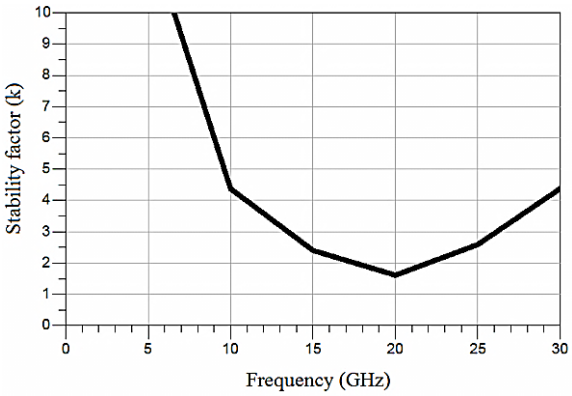


Fig. 8. Simulated stability factor (k) of the proposed CMOS-DA

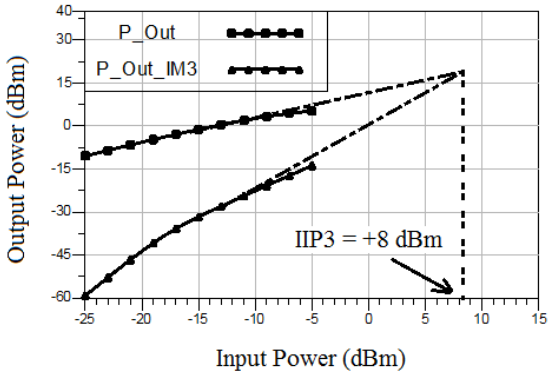


Fig. 9. Simulated fundamental and IM3 output power versus input power characteristics at 15 GHz

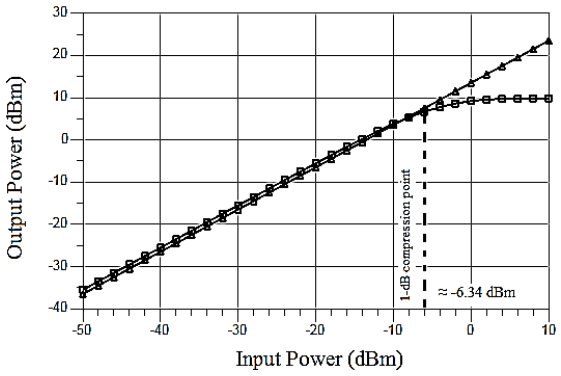


Fig. 10. Simulated input referred 1-dB compression point at 15 GHz of the proposed CMOS-DA

To date, the various methods have been presented to improve the DA design parameters. To evaluate the efficiency of each new design, a figure of merit (FoM) is needed. One FoM included the most relevant parameters such as low-power, high-gain, low-noise, and broad bandwidth can be given as Eq. (24) [8]:

$$\text{FOM} = [\text{GHz/mW}] = \frac{S_{21}[1]\ \text{BW[GHz]}}{(\text{NF}-1)[1]P_{DC}[\text{mW}]} \quad (24)$$

Where S_{21} [1] refers to the average power gain in magnitude, BW [GHz] mentions the 3-dB bandwidth in gigahertz, (NF - 1) [1] is the excess NF in magnitude and P_{DC} [mW] demonstrates power consumption in milli watts.

The comparison results of the proposed CMOS-DA with those of recently published CMOS-DAs are summarized in Table 1. The good value of the proposed DA's FoM confirms that the proposed DA well can satisfy the important design parameters which DA and LNA designs are faced with them while its ultra-broad bandwidth and high input third intercept point are highly desired. The proposed CMOS-DA comparing with the other published work achieves a good performance for ultra-broadband amplification applications.

The MC simulation is an appropriate option to take into consideration the risks associated with various input parameters which they receive little or no consideration in simulating of designs utilizing ideal components. MC simulation is a technique to understand the impact of inputs' uncertainty on the overall performance of the design. It works based on a repetitive process including a random value selection for input parameters within their specified tolerance range and getting a set of output parameters as a result of multiple trial runs [18]. Uncertainty inputs in the proposed design are device variations including fluctuations in MOS parameters such as effective gate length L_{eff}, threshold voltage V_{th}, thickness of the gate oxide T_{ox}, and the drain-source region parasitic resistance R_{dsw} [19]. Not only MOS device variations are considered, but also the effects of supply voltage and passive component tolerances are taken into account. In MC simulation, the proposed design is simulated a large number of times (e.g., 1000). For each run, all of the uncertain parameters are sampled. ADS software package can generate uniformly distributed random values of parameters, which a normal (Gaussian) distribution is used in this design. Note that the Gaussian distribution models the worst case of possible situation. The circuit is then simulated. As a result, actual observations of failures are routinely better predicted by the MC simulation results. In this way, we are beginning to understand the risk and uncertainty in the proposed design.

Figs. 11 ~ 13 show the trend of the influence of MOS device, supply voltage variation, and passive component tolerances on proposed design's performance.

Here, performance refers to S-parameters NF and stability-factor responses. The fluctuations of MOS parameters belonging to 0.13 µm CMOS technology are given according to Table 2 [24].

The result of mentioned variations on power gain of the proposed design is shown in Fig. 11 (a). As it can be seen, the density of results around of 14 dB validates the accuracy of power gain response. As it is shown in Fig. 11 (b), the revers isolation achieves very good values within total MC trial to that of ideal simulated revers isolation. Also, both input and output impedances matching within total MC trial are better than - 15 dB according to Figs. 12 (a) & 12 (b) which they imply that the good impedances matching are yielded. NF response is shown in Fig. 13 (a) that confirms the values of this factor are between 3 to 4 dB within total MC trial. Finally, Fig. 13 (b) illustrates the stability-factor response of the MC simulations. It guarantees that the proposed design is unconditionally stable under whole situation.

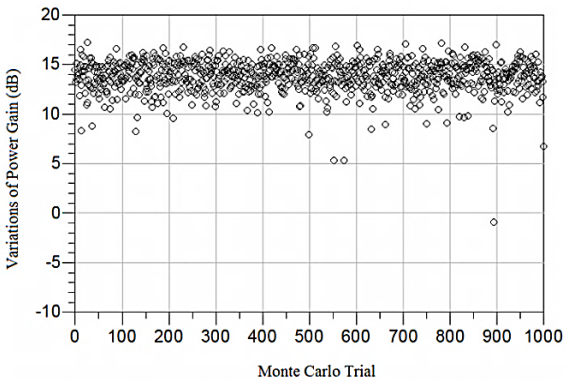
Table 1. Recently reported state-of-the-art CMOS-DAs versus the proposed CMOS-DA

References	Process	Freq (GHz)	Gain (dB)	Average NF (dB)	S11 (dB)	S22 (dB)	PDC (mw)	FOM (GHz/mW)
[9]2013a	0.18µm CMOS	32	9.5	5.85	<-15	<-10	71	0.44
[5]2011a (HG mode)	0.18µm CMOS	1.5~8.2	17.1 ± 1.5	3.52	<-11	<-10.1	46.85	0.7
[5]2011a (LG mode)	0.18µm CMOS	1.2~ 8.6	11.4 ± 1.4	3.74	<-9.4	<-10.4	9.85	1.72
[2]2011a	0.18µm CMOS	35	20.5	7.4	< -12	< -14	250	0.34
[15]2013b (HG mode)	0.13µm CMOS	0~11	20.5 ± 0.5	6.5~8	<-11	<-18	9.36	2.95
[15]2013b (LG mode)	0.13µm CMOS	0~12	15.5 ± 0.25	6~8	<-11.5	<-16.5	3.6	5
[7]2011b (HG mode)	0.13µm CMOS	0.4~10.5	20.47 ± 0.72	3.29	<-10	<-10	37.8	1.73
[7]2011b (LG mode)	0.13µm CMOS	0.7~10.9	11.03 ± 0.98	4.25	<-10.3	<-10.9	6.86	2.67
[8]2015b	0.13µm CMOS	DC ~ 13	26.5 ± 0.4	5.4	<-11.1	<-11.3	9.95	10.2
This workb	0.13µm CMOS	DC ~ 23	14.2 ± 0.5	3.65	< -10	< -10	45.63	1.96
This workc	0.13µm CMOS	DC ~ 23	14 ± 1.5	< 4	< -20	< -15	< 50	~ 1.9

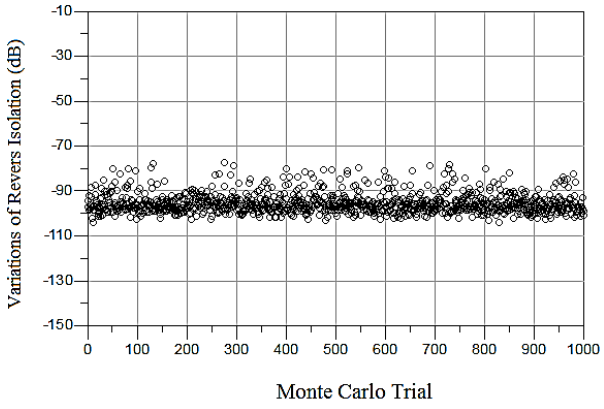
a: Based on the measurement results b: Based on the simulation results c: Based on the MC simulation results

Table 2: Parameter Values and ±3σ Variations of MOS transistor [24]

Technology	**0.13 µm**	
Parameters	**nmos**	**pmos**
$\mathbf{L_{eff}(\mu m)}$	0.09 ± 15%	0.09 ± 15%
$\mathbf{T_{ox}(A^0)}$	33 ± 4%	33 ± 4%
$\mathbf{V_{th}(V)}$	0.33 ± 15.5%	- 0.33 ± 15.5%
$\mathbf{R_{dsw}(\Omega/m)}$	200 ± 10%	400 ± 10%
$\mathbf{V_{dd}(V)}$	1.3 ± 10%	

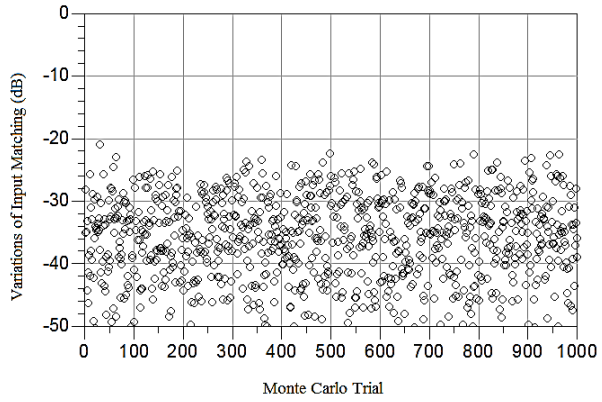


(a)

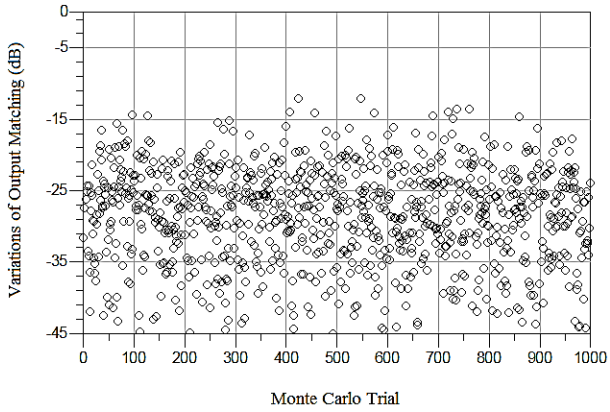


(b)

Fig. 11. Scatter plot of 1000 Monte Carlo runs for investigating a) Power Gain and b) Reverse Isolation Performances

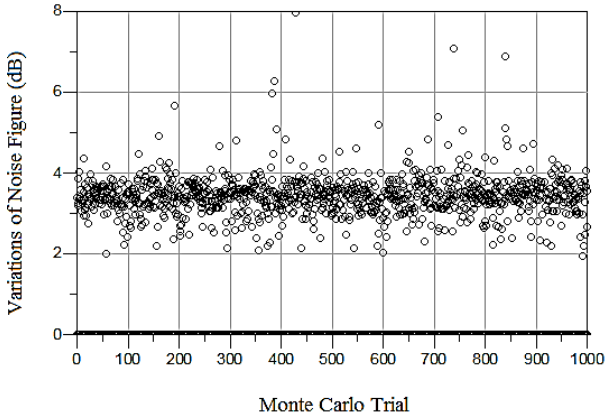


(a)

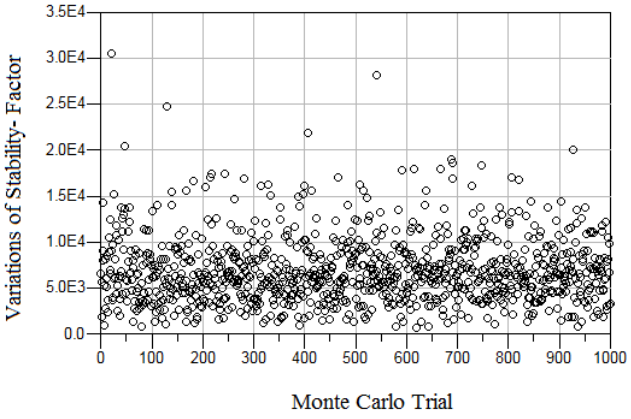


(b)

Fig. 12. Scatter plot of 1000 Monte Carlo runs for investigating a) Input Matching and b) Output Matching Performance



(a)



(b)

Fig. 13. Scatter plot of 1000 Monte Carlo runs for investigating a) Noise Figure and b) Stability-Factor Performances

4. Conclusions

In this study, a high-performance CMOS-DA construction using a new gain-cell has been reported. The new gain-cell combining the regulated cascode, and inductively coupled cascode techniques has been removed the shortcomings of both cascade gain-cells including restricted bandwidth and cascode gain-cells consisting limited signal swings to yield a significantly broadband CMOS-DA. The simulated results of the gain, input and output return losses, isolation, and NF have been illustrated the capability of utilizing this device for ultra-broadband amplification applications. It has been demonstrated promising solution over the previous reports to realize the balanced trade-off between critical challenges facing design of DAs. The effect of parameters variation on performance specifications of the proposed design has been simulated by MC simulation which it was confirmed MC and ideal simulation results are in a good agreement.

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Zainab Baharvand received her M.Sc degree in Electrical Engineering at the Graduate University of Advanced Technology, Kerman, Iran. Now her research interests include design of RF building blocks for ultra-broadband applications. The focus of her research is on design of distributed amplifier (DA) and variable gain distributed amplifier (VGDA) in 0.13 μm CMOS technology.

Ahmad Hakimi was born in Rafsanjan, Iran, in 1961. He received the B.Sc degree in electrical engineering from Technical College of Shahid Bahonar University of Kerman, Kerman, Iran, in 1986. Using the scholarship, which was granted by the Ministry of Higher Education of Iran and Istanbul Technical University (ITU) in 1987, he has been studying for the degree of M.Sc and Ph.D in the faculty of electrical and electronic at the ITU. He received the M.Sc and Ph.D degrees from ITU in 1995 and 1996 in the field of high-frequency electronics. His research interests include the design and analysis of nonlinear RF circuits, numerical analysis and advanced engineering mathematics, analog filter design and Industrial Research Center, Kerman, Iran, and Department of Electrical Engineering, Shahid Bahonar University of Kerman, Kerman, Iran.